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PHASE II FINAL DEVELOPMENT REPORT FOR HIGH-RELIABILITY, LOW-COS--ETC(U)
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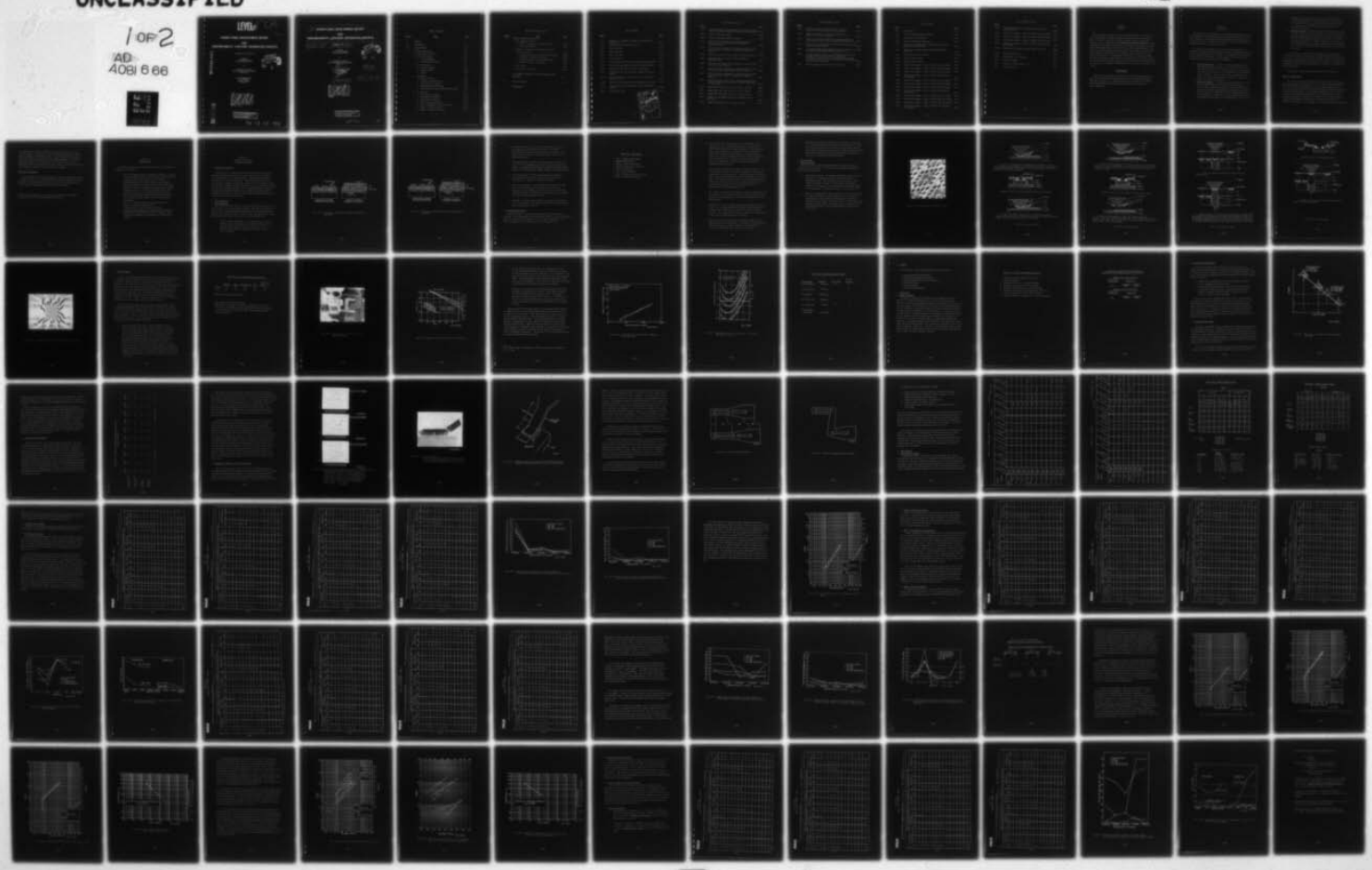

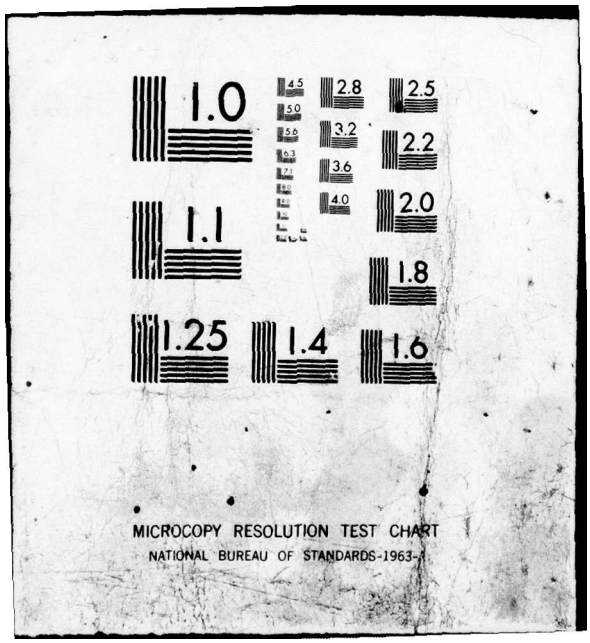
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PHASE II FINAL DEVELOPMENT REPORT

FOR

HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS

3 FEBRUARY 1977 TO 22 MAY 1979

Prepared By
RCA Solid State Divison
Route 202, Somerville, N.J. 08876

For

DEPARTMENT OF THE NAVY
NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D.C.

Contract No. N00039-76-C-0240
Project No. 62762N
Subproject No. XF54586
Task No. 002

(6)

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SECTION I

ABSTRACT

The objectives of Phase II of this investigation were to fabricate significant quantities of eight integrated circuit types using the techniques defined in Phase I (see Phase I Final Development Report for High Reliability, Low Cost Integrated Circuits, ~~Contract No. N00039-76-C-0240~~), perform a preliminary reliability investigation, and formulate comparative cost data. Wafers and finished devices were processed for eight integrated-circuit types. These types included three TTL circuits (5420, 5472, 5470), one Schottky TTL circuit (54S20), three CMOS circuits (CD4012B, CD4014A, CD4027A) and one linear circuit (CA741). The preliminary reliability investigations defined potential reliability problems, which were subsequently successfully resolved, and provided preliminary data regarding activation energies and failure rates. The comparative cost analysis indicated that the cost goal of the contract can be met.

ACKNOWLEDGMENT

Support for this program was provided to the RCA Solid State Division by the Naval Electronics Systems Command, Electronics Technology Division, ELEX 304, Washington, D.C. Technical direction was provided by the Naval Ocean Systems Center, Advanced Applications Division, Code 923, San Diego, California.

SECTION II
INTRODUCTION

The objective of this program is to investigate alternate approaches to MIL-M-38510 for producing high-reliability integrated circuits at low cost. Emphasis is on adapting existing technology to industry mainstream products to achieve a semiconductor reliability which will meet military requirements without a severe cost penalty.

The approach to achievement of the goals of this program is the integration and application of existing sealed-chip integrated-circuit processing with automated plastic packaging. The program will be carried out in three phases. During Phase I of the program - Sealed-Chip Process Utilization - three major tasks were accomplished:

(a) Process feasibility - in which the required photomasks were generated using existing masks to the maximum extent possible. Then, small quantities of each device type were made to assure that the masks and processes were available for the production runs of Phase II. Also, each device type was made using a matrix of carefully varied process parameters to assess their impact on yields and reliability.

(b) Process development - in which the processes required to fabricate the eight integrated-circuit types to be produced in Phase II were defined and documented. Silicon nitride passivation and the titanium-platinum-gold metallization system were used to achieve chip "hemeticity" and a corrosion-free metallization system. In addition, a silicon nitride overcoat layer was applied for protection of the metallization. A series of

experiments was carried out at each critical processing step to assure repeatability. Real-time indicators and accelerated life tests were used to assess the effects of process changes on reliability and to measure progress in achieving the required failure rate.

(c) Automated assembly - in which the assembly technology to be used in Phase II was defined and documented. The effect of assembly process parameters on cost and yield was assessed. Bonding tapes and lead-frames compatible with each of the device types were designed and fabricated. A number of devices of each type were then assembled using the automated assembly system. Reliability was continually monitored by real-time indicators and accelerated life tests.

At the conclusion of Phase I, the photomasks, wafer process and assembly process required to fabricate the eight integrated-circuit types in the low-cost high-reliability device-fabrication phase were defined and documented,and sample devices of each type were fabricated. Additionally, preliminary reliability data were generated to demonstrate the soundness of the chosen approach.

At this time, the production runs of Phase II were undertaken.

Phase II - Fabrication

The low-cost high-reliability device-fabrication phase of the program involved significant quantities of each of the eight selected integrated-circuit types fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits were constructed in both plastic and ceramic packages. This arrangement permitted a comparison to be made of the new and conventional processes and provided the control units required for the Phase III reliability evaluation. The utilization of existing equipment and mask sets

was demonstrated, and the cost impact of converting to this type of processing estimated. Preliminary reliability testing highlighted two problem areas, Cu migration and beam-tape stress. Modifications to the packaging system were made which successfully resolved these problems.* All devices produced in Phase II of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program have been defined and assembled.

Phase III - Reliability

The reliability of the devices produced in Phase II will be demonstrated. In addition, the level of testing required over and above commercial screening to assure a reliable product for military end use will be determined, and the cost impact of this testing will be analyzed and verified.

*Constant-stress testing has been utilized to determine the reliability potential of two of the eight integrated-circuit types.

SECTION III
ACCOMPLISHMENTS

Conclusions derived from the work during Phase II of the program may be summarized as follows:

- The silicon nitride trimetal (Ti-Pt-Au) technology is adaptable to the form (CMOS, T^2L, Schottky T^2L, bipolar linear) types of integrated circuits fabricated under this contract.
- Plasma-deposited silicon nitride overcoat layers provide improved resistance to sodium penetration over CVD PSG films.
- Copper beam tapes in conjunction with expoxy novalac molding compounds can lead to a long-term, high-temperature failure mechanism because of copper dissolution and redeposition.
- Beam-tape designs which incorporate stress-relief features are essential to provide highly reliable chip/lead-frame interconnects.
- The use of a silicone molding compound on HRLC devices provides a reliable packaging system.
- A burn-in screen for HRLC devices was defined.
- A wafer-to-wafer reliability difference has been identified.
- HRLC devices can be fabricated at a cost increase of less than 20% over commercial high-reliability plastic-packaged devices.

SECTION IV

DETAILED FACTUAL DATA

TECHNICAL DISCUSSION

A. Objectives of Phase II

During Phase II of this program to design and develop low-cost high-reliability integrated circuits, four major tasks have been performed, (1) Wafer Fabrication, (2) Device Assembly, (3) Preliminary Reliability Assessment, and (4) Cost Verification. Wafer Fabrication produced the die required to assemble a significant quantity of each of eight integrated-circuit types. Assembly and Test completed the devices required for delivery and Phase III reliability testing. The Preliminary Reliability Assessment has gauged the reliability potential of the HRLC levels and uncovered assembly-related problems. The Cost Verification task demonstrated the cost increment associated with HRLC devices.

B. Wafer Fabrication

1. Process Elements

HRLC wafer fabrication differs from conventional processing only in the latter phases of the wafer-processing sequence. Diffusions are identical to those used for aluminum metallized non-silicon-nitride-passivated devices, although oxide thickness differs in certain cases. The key elements of HRLC wafer processing are shown in Fig. IV-1, and are described below.

a. Silicon Nitride Passivation - at the completion of the wafer diffusion cycles, a chemically vapor-deposited (CVD) silicon nitride film is utilized to seal the wafer. This film is moisture and alkaline-ion resistant and provides enhanced device stability.

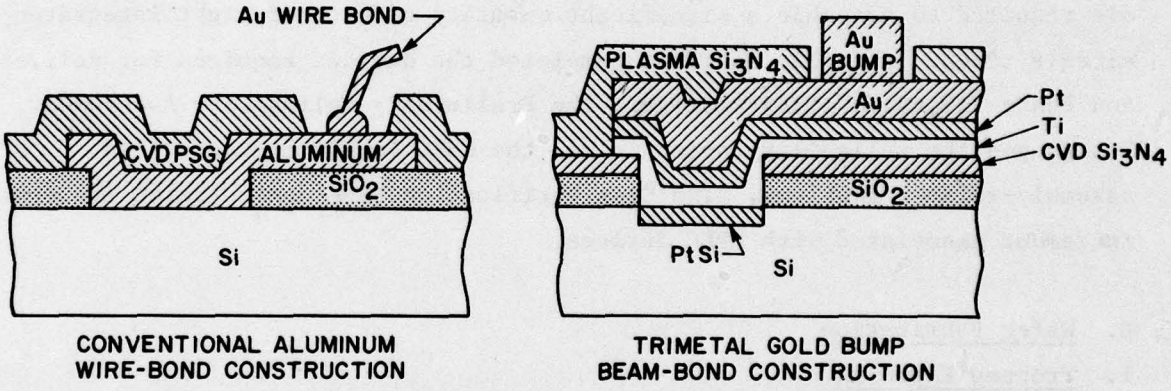


Fig. IV-1 - Comparison of aluminum and trimetal interconnection structures.

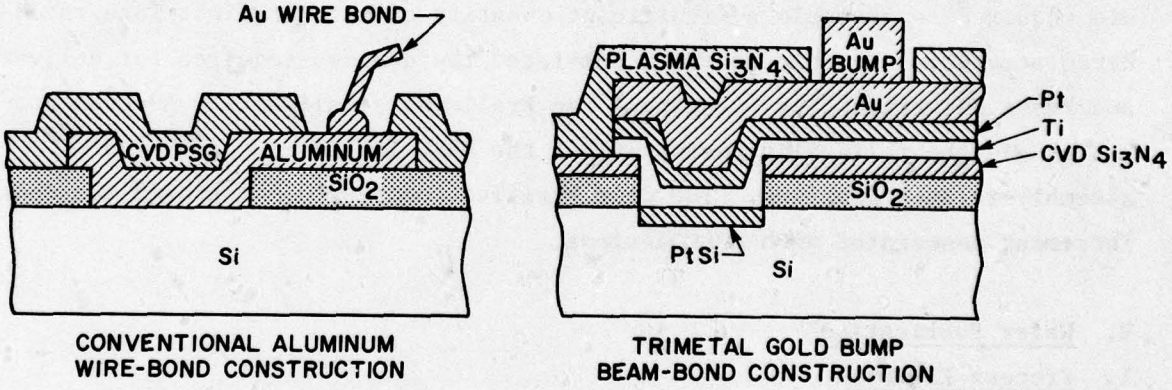


Fig. IV-1 - Comparison of aluminum and trimetal interconnection structures.

b. Platinum Silicide - after the contact opening step, a thin film of platinum is sputtered onto the surface of the wafer. A high-temperature sintering step forms platinum silicide in the contact areas to provide low resistance ohmic contacts to the underlying silicon.

c. Titanium/Platinum - Titanium is sputtered onto the surface of the wafer to provide adherence between the CVD Si_3N_4 and subsequent layers. The sputtered platinum layer provides a diffusion barrier between the titanium and the primary conductor, electroplated gold.

d. Gold Interconnects - the main current-carrying constituent of of the metallization system is gold, which is selectively electroplated to complete the interconnect system.

e. Plasma Silicon Nitride - the metallization overcoat of the HRLC wafers is plasma-deposited silicon nitride, which adheres tenaciously to the underlying surfaces because of its internal compressive stresses. It provides a barrier against the formation of electroplated-gold migrative shorts.

f. Gold Bump - Gold bumps .001-inch high are plated in the bond-pad areas of the wafers. These bumps facilitate the beam-tape bonding used to assemble HRLC devices.

2. Technology Application

Wafer fabrication of the eight integrated-circuit types has been completed. HRLC processing has been successfully adapted to four technologies, CMOS, T^2L, Schottky T^2L and bipolar linear, as shown in Table IV-1. The wafer processing for each technology is briefly discussed below.

Table IV-1 - HRLC Devices

- CA741 - Bipolar Linear OpAmp
- CD4012UB-CMOS NAND Gate
- CD4014A - CMOS Shift Register
- CD4027B - CMOS Dual J-K Flip Flop
- 5420 - T^2L NAND Gate
- 5470 - T^2L J-K Flip Flop
- 5472 - T^2L Master Slave J-K Flip Flop
- 54S20 - Schottky T^2L NAND Gate

a. CMOS - Processing of CMOS wafers for the HRLC program is conventional up to the channel-oxidation step. At this point a thinner-than-normal channel oxide is grown so that the composite SiO_2 - Si_3N_4 dielectric is equivalent in terms of threshold voltage to a conventional SiO_2 dielectric. Metallization of these wafers utilizes magnetron-sputtered titanium and platinum and electroplated gold. Electrical characteristics of HRLC devices are equivalent to those observed on conventional aluminum-metallized devices.

The processing of CMOS wafers results in tapered oxide cuts. It was found that this type of geometry is amenable to sputter-etch techniques for metal definition. Accordingly, sputter etching was used to define the platinum film using the plated gold as a sputter mask. This technique obviates the need for the platinum-definition photoresist step and allows the use of tightened design rules to increase packing density. This development indicates the applicability of HRLC processing to LSI.

b. T^2L - HRLC processing has been found to be entirely compatible with T^2L technology. No deleterious effects of the CVD silicon nitride deposition or metallization on any electrical characteristics has been observed.

c. Schottky T^2L - The use of HRLC technology on Schottky T^2L circuits results in the clamping diode being formed of platinum silicide. In conventional structures, this device is formed by aluminum silicide. This change did not impact the electrical characteristics of the circuits fabricated under the contract.

d. Bipolar Linear - HRLC processing is completely compatible with bipolar-linear wafer fabrication. No variations from conventional wafer processing are required through the emitter-diffusion process, at which point HRLC processing is initiated.

Independent of whether the devices are conventional or HRLC, the use of a surface-field ion implantation has been found to be useful in raising the field inversion voltage of the collector regions. This condition precludes the formation of conductive p-type channels between base regions and isolation regions when the devices are operated from relatively high-voltage supplies.

C. Device Assembly

1. Beam-Tape Bonding

HRLC devices are assembled using semiautomated gang TC bonding to a continuous reel of beam tape. This procedure is accomplished through the following process sequence:

a. Lamination Separation - the thinned, electrically tested wafers are laminated to a supportive substrate through the medium of a paraffin-based wax. The individual die are separated by sawing completely through the wafer. At this point, the substrate maintains the integrity of the chip matrix for inner-lead bonding. As SEM photograph of a sawed wafer array is shown in Fig. IV-2.

b. Bonding - the sawed wafer array is mounted on a precision X-Y table for inner-lead bonding. The beam tape, which has a unique beam configuration for each bond-pad configuration, is loaded and threaded into the machine. The entire inner and outer lead-bonding sequence is shown in Figs. IV-3 through IV-6. A photograph of an IC assembled by means of the automated assembly system is shown in Fig. IV-7.

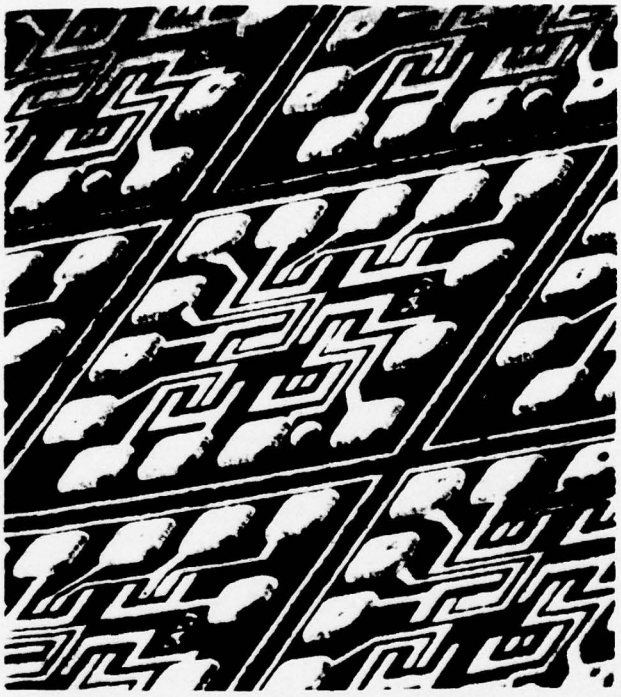
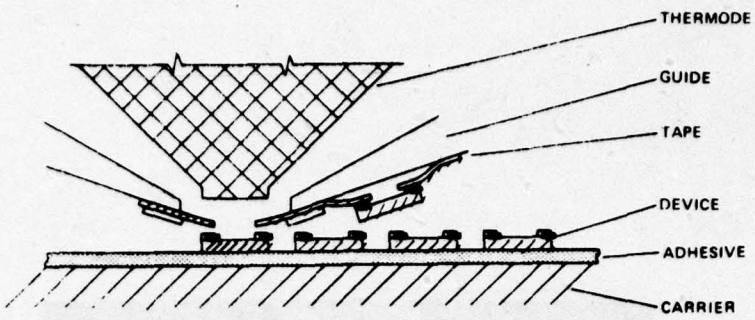
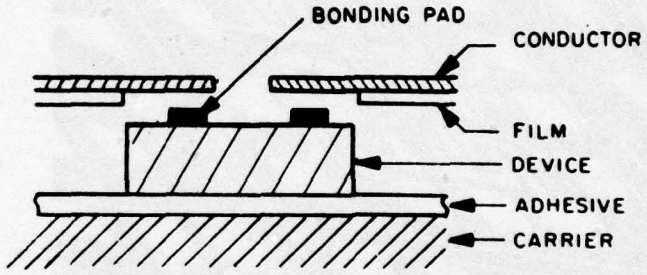


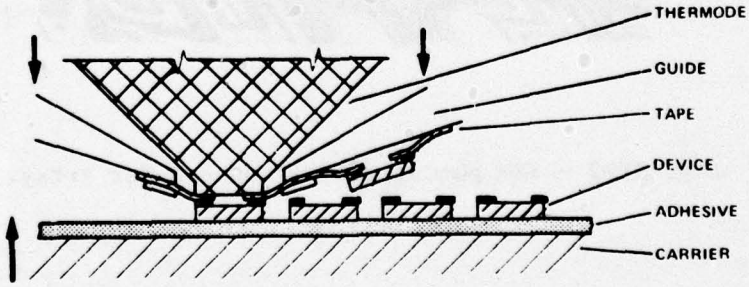
Fig. IV-2 - SEM photograph of sawed wafer array.



1. ALIGN - in this system the thermode is the reference. Devices are automatically pre-aligned by the precision X-Y table. To compensate for manufacturing variables in the tape, it is manually aligned with the device during each cycle by the operator.

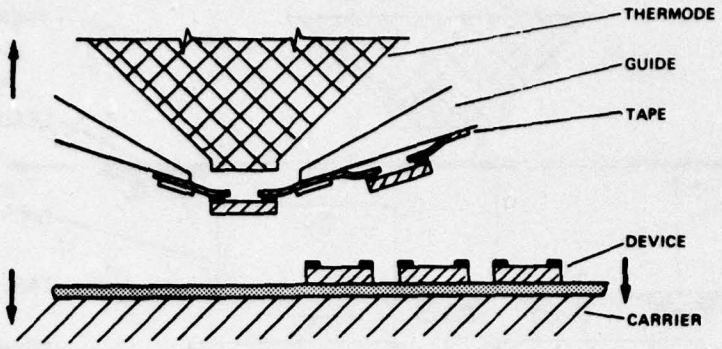


Magnified View of the tape fingers and device after alignment.

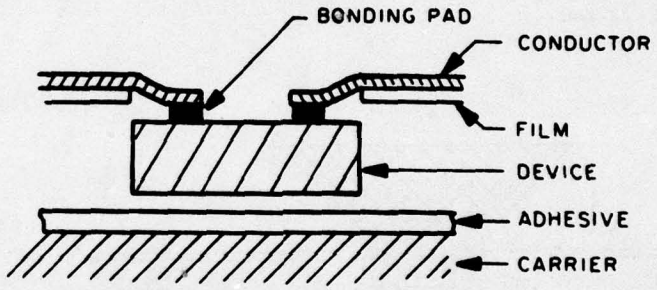


2. BOND - The device carrier rises to the bond level and the thermode moves in and down to apply heat and pressure through the metallic fingers on the tape to the bond pads on the device.

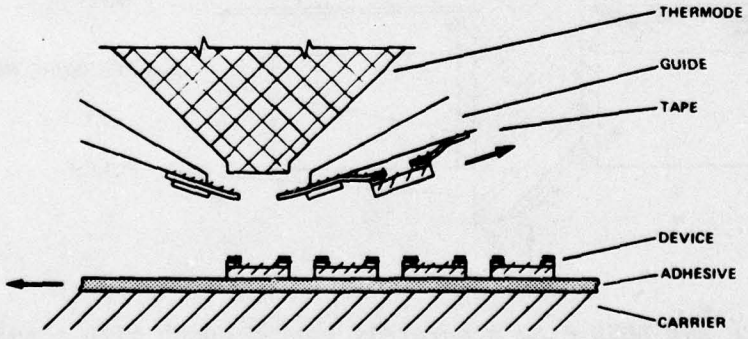
Fig. IV-3 - Inner lead bond.



3. PICK - At the completion of the preset bond cycle, the thermode retracts; as soon as the thermode is clear of the tape, the device carrier retracts to provide clearance so that the tape can index to carry the finished part away.

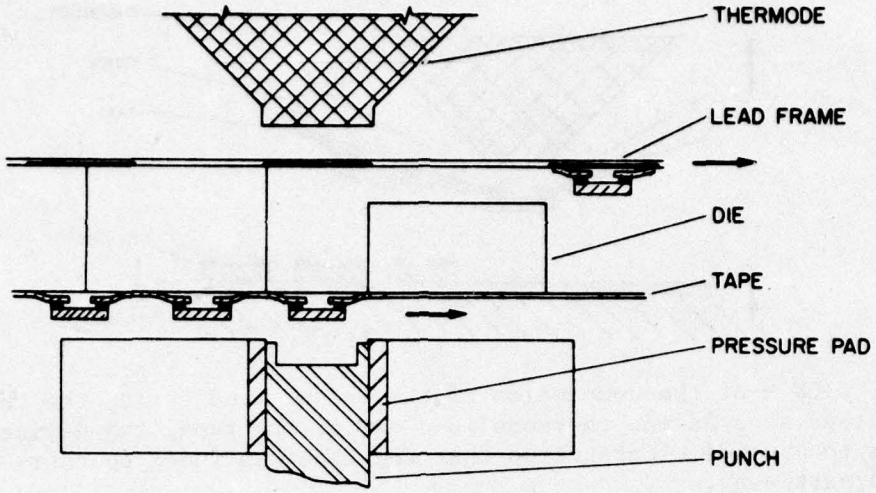


Magnified view of the tape fingers and device after bonding

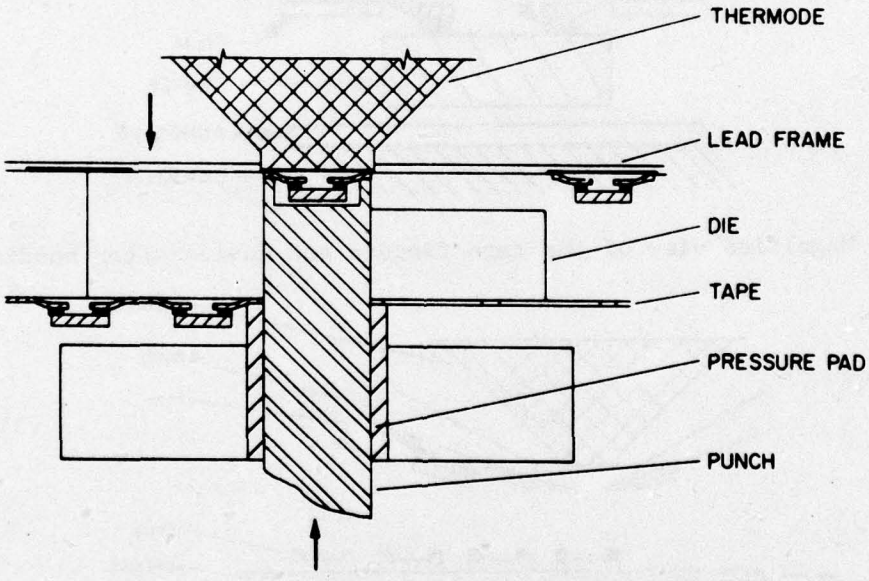


4. FEED - The tape indexes to remove the completed part and position a fresh tape frame for the next bond. Also, the X-Y table indexes to position a new device. At the completion of the feed indexes, the device carrier rises to the align position.

Fig. IV-4 - Inner lead bond.

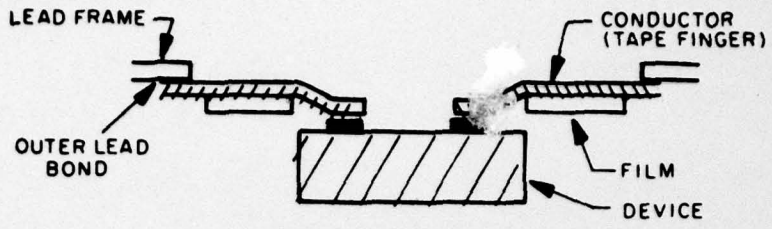


5. FEED - Precision feed mechanisms advance both tape and lead frame.

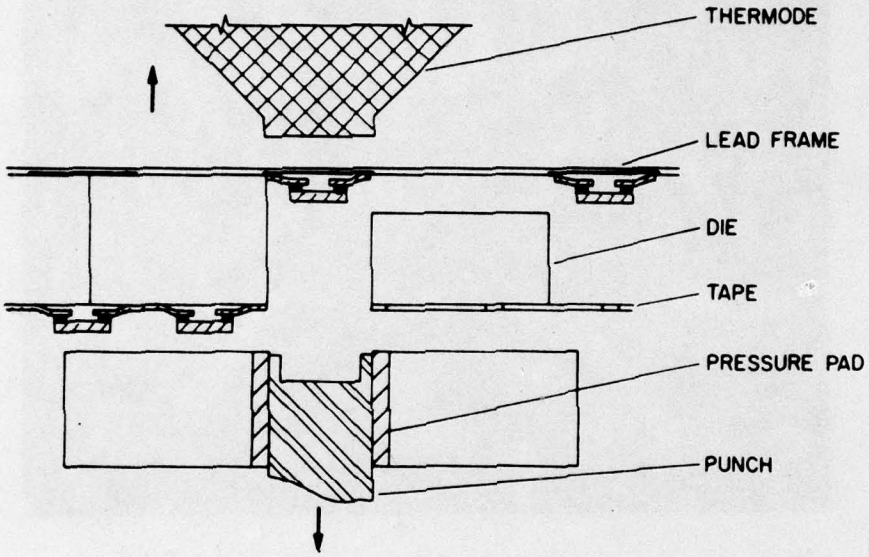


6. PUNCH AND BOND - An accurately fitted punch with a spring-loaded pressure pad cuts the device and its leads from the tape and carries it up through the die plate until it contacts the lead frame. At that time the thermode commences its down stroke and applies the heat and pressure to form the bond through the lead frame using the punch as the bond anvil.

Fig. IV-5 - Outer lead bond.



Magnified view of the completed assembly.



7. RETRACT - Punch, pressure pad and thermode retract ready for the next part index.

Fig. IV-6 - Outer lead bond.

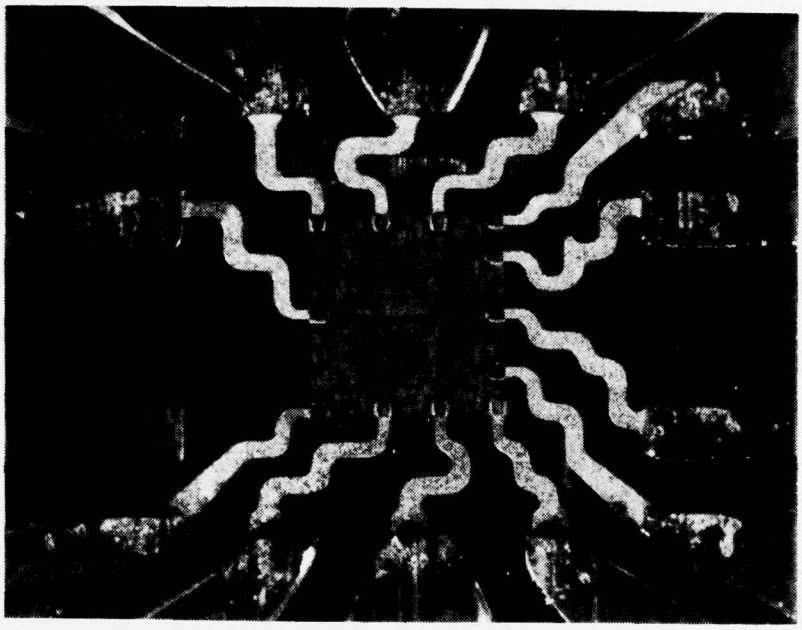


Fig. IV-7 - IC assembled by means of the automated assembly system.

2. Molding Compound

In order to attain the cost/reliability goals of this program, the use of commercial molding compounds for the dual-in-line plastic-packaged devices is required. The test cells that were initially evaluated are shown in Table IV-2. The results of this testing showed an electrical shorting failure mechanism for the cell using epoxy molding compound, Fig. IV-8. All of the devices using silicone molding compound showed parametric degradation, but no units became inoperative. It was initially postulated that the shorts occurring at the high temperature in the epoxy cells would only occur at temperatures of 175°C to 200°C. However, extension of the 150°C test time to 4000 hours, Fig. IV-9, produced the same failure mechanism.

These data indicated that with the beam-tape package system, certain epoxy-molding compounds, with or without a silicone junction coat, caused a shorting mechanism, as described below, close to the 125°C rating of the device. The use of epoxy would preclude any use of specific high temperature burn-in conditions as part of a screen to remove infant mortality, which usually impacts early system life. Use of epoxy would also be a reliability hazard of some degree even for 125°C ambient operation.

a. Failure Mechanism - The unique failure mechanism which was observed was associated with a corrosive attack by constituents of the particular epoxy molding compound used, at temperatures equal to or greater than 150°C, upon the structural components of the metal support structure of the semiconductor device. The conductive metallic-copper paths that are created at these temperatures between oppositely biased conductors result in electrical shorts. The actual mechanism of copper going into solution is not well known, but it is independent of the presence of electrical bias. The bias does, however, cause the preferential conductive paths to occur. Fig. IV-8 is a photograph of the copper shorting mechanism between the beams of the inner bond connections of the chips.

Table IV-2 Initial Molding-Compound Evaluation

	Silicone	Epoxy	Epoxy with JC	DIC*	Nonhermetic DIC**
CD4012	195	195	195	145	145
CA741	195	195	195	145	145

Numbers indicate device quantities.

*DIC = Dual In-Line Ceramic Package

**Nonhermetic DIC package is attained by providing a hole in the metal lid of the package, thereby admitting the ambient environment but preventing the possibility of damage through handling during testing operations.

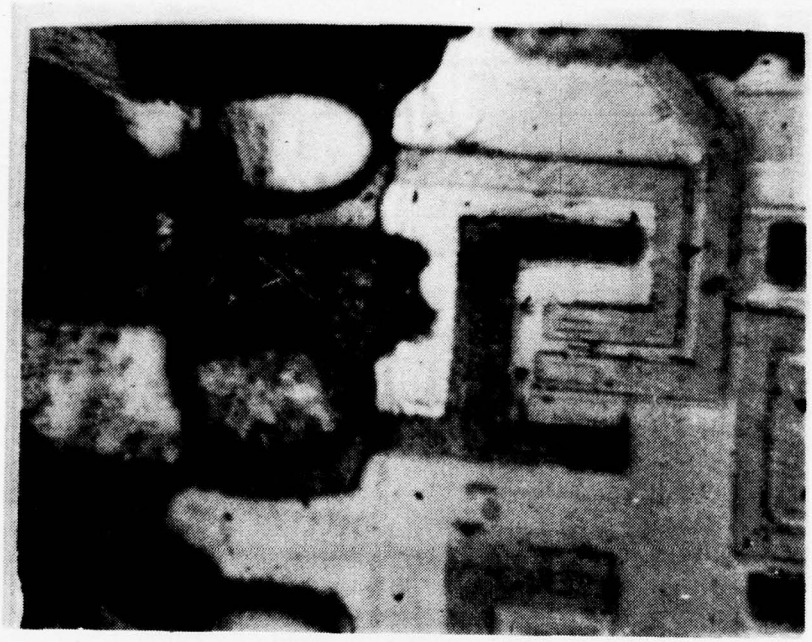


Fig. IV-8 - Copper shorting mechanism for epoxy molding compound.

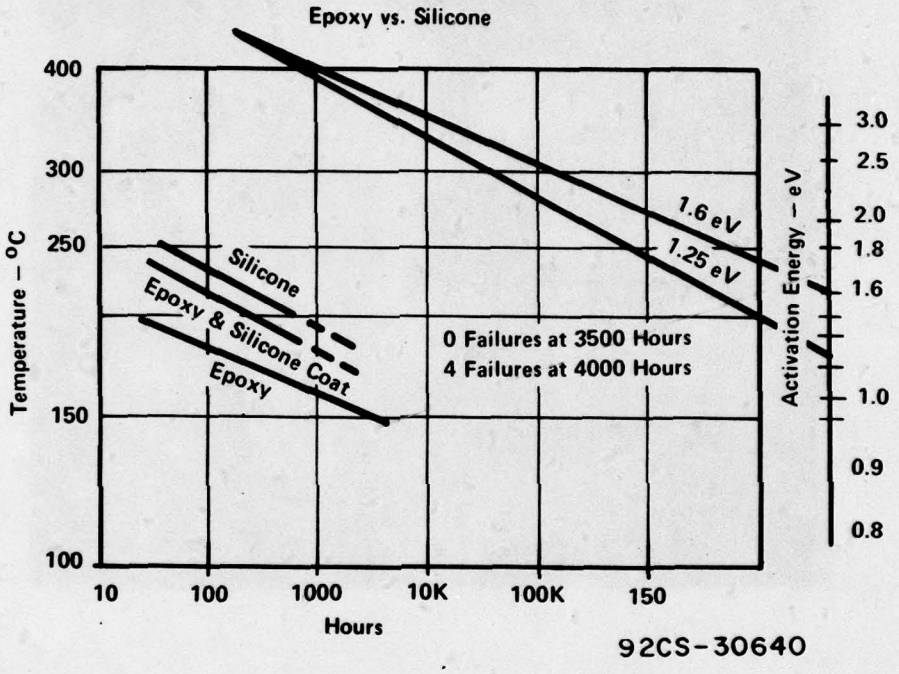


Fig. IV-9 - Extension of the 150°C test time to 4000 hours.

b. Data on Silicone Molding Compound - The accelerated life tests on the silicone molded devices caused no inoperative-type failures at 250°C bias under static-life conditions. Fig. IV-10 shows a log-normal plot for the CA741 to 2,400 cumulative hours using commercial limits. No metallurgical or materials problems were made evident by electrical measurements. Most devices that exhibited large shifts in characteristics recovered with baking of the devices.

Assuming a 1.74 electron-volt activation energy, Fig. IV-11 shows the median life required as a function of the standard deviation at 250°C to predict the failure rate at 125°C. The standard deviation for the data shown in Fig. IV-10 is 4. Therefore, from Fig. IV-11, an MTF of 50,000 hours at 250°C would be required to predict the failure rate specified (0.005%/1000 hours or 50 FITS*) at 125°C.

One reason for the difficulty caused by the silicone molding compound in commercial devices is the stress on wire bonds and the effects of salt penetration into the package. In the HRLC system, wire bonds are not used, and the semiconductor chip is of the sealed-junction type with a thermal silicon nitride passivating layer. The glassivation system is a plasma-deposited low-temperature nitride, which is an additional barrier to the passage of alkali metals. Table IV-3 shows the results of two extremely severe sequences of reliability tests performed to demonstrate the capability of the HRLC product using the silicone molding material when exposed to highly contaminated environments. The ability of the silicone-molded devices to survive these sequence tests is clear.

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*FIT = Failure Unit = one Failure in 10^9 device hours (e.g. 0.0001%/1000 hrs. = 1 FIT)

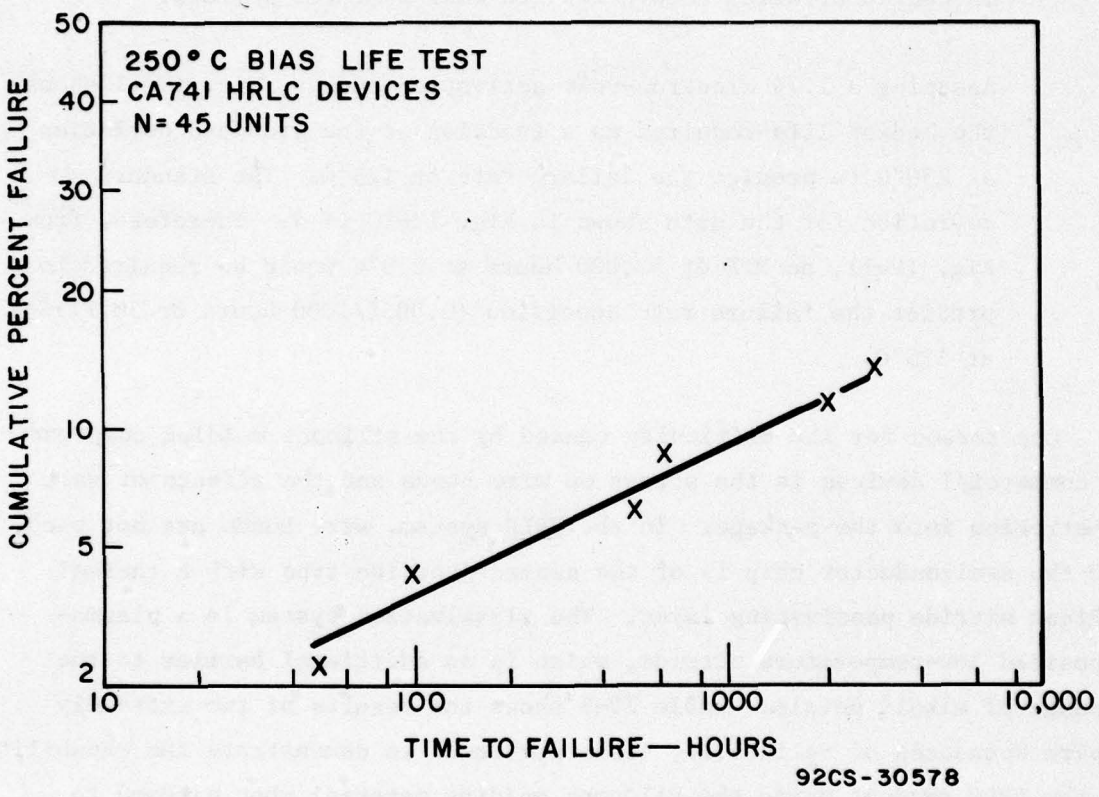

Fig. IV-10 - A log-normal plot for the CA741, commercial electrical limits.

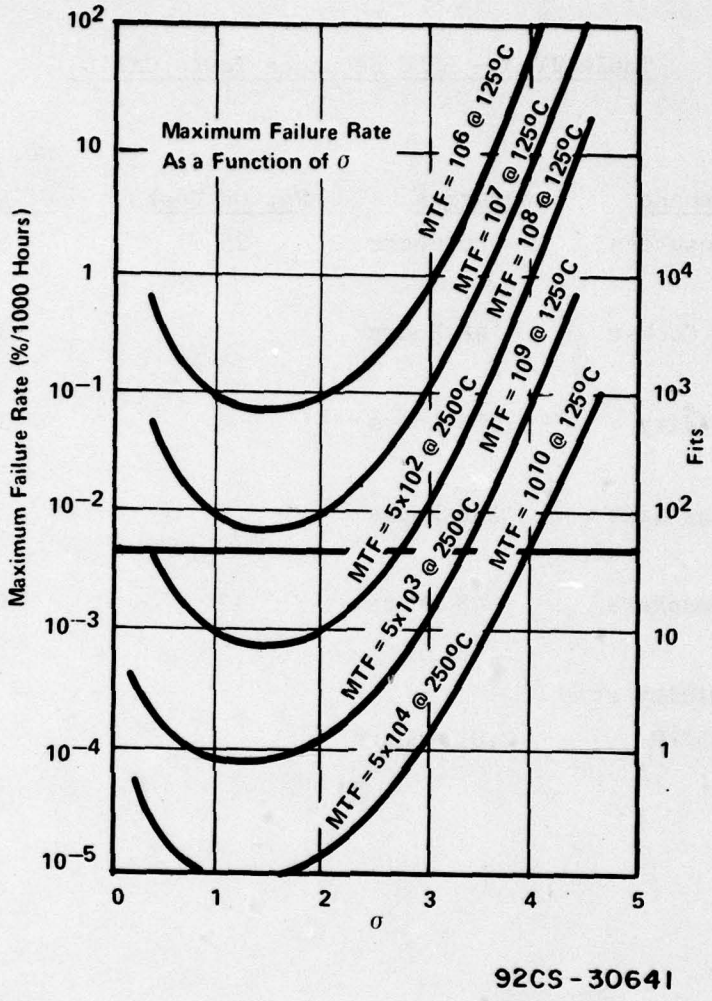

Fig. IV-11 - Peak failure rate as a function of σ for various MTF with E_A = 1.7 eV.

Table IV-3 - HRLC Sequence Tests CA741G

Test Sequence	Duration	No. On Test	No. Out Of Spec.
Salt Atmosphere	96 Hours	25	0
+			
Pressure Cooker	48 Hours		1
+			
Bias/Humidity	1,008 Hours		1
+			
250°C Bias Life	168 Hours		5
Salt Atmosphere	48 Hours	12	0
+			
Bias/Humidity at 85°C/85%RH	2,012 Hours		0

3. Summary

The attributes of HRLC integrated circuits are as follows:

- Silicon nitride chip passivation
- Titanium-platinum-gold metallization
- Plasma-deposited silicon nitride overcoat
- Gold bonding bumps
- Beam-tape bonding
- Silicone molding compound

D. Reliability

1. Phase II Program

The Phase II reliability objectives of this program are shown in Table IV-4. Quantitative results for all of these factors have been defined. Rather than using generic definitions as criteria for failure rates, activation energy, failure mechanism, and burn-in (the definitions normally used for commercial and military product), the Phase II program was designed to provide specific information on the HRLC product. The main intent from the viewpoints of cost-effectiveness and reliability is to determine the most accurate available method of estimation of reliability by testing to conditions close to actual functional usage, but under accelerated ambient conditions. Long-term testing at rated conditions of the HRLC product would supply the most reliable results for a failure-rate calculation, but the cost would be excessive (Table IV-5). Moreover, the most probable cause of field failures might not be determined since all failure mechanisms would probably not be found, even under long-term conditions.

Table IV-4 - Phase II Reliability Objectives

1. Determine activation energy as function of failure definition
2. Determine if there is an activation energy difference for infant and central failures
3. Estimate infant mortality for each temperature
4. Determine feasibility of high-temperature burn-in in place of conventional 125°C, 168-hour burn-in
5. Perform preliminary determination of failure mechanisms

Table IV-5 - Sample Plans to Demonstrate
0.005%/1000 Hour Failure Rate with 125°C Life Test

8000-Hour Test 90% Confidence		
Failure Rate %/1000 Hours	Sample Size	
	0 Failure	1 Failure
0.005	5600	9400

8000-Hour Test 60% Confidence		
Failure Rate %/1000 Hours	Sample Size	
	0 Failure	1 Failure
0.005	2300	5000

2. Reliability Demonstrations

A wide gap frequently exists between the ability to relate the chemical and physical properties of materials to electrical characteristics of components and their behavior on life test or in aging environments. There are two basic methods of generating data for predicting or estimating failure rates of components:

1. Conduct static long-term life tests that simulate some aspects of the component's actual application.
2. Conduct short-term accelerated tests that excite the mechanisms of failure most likely to occur. These data are then extrapolated by equation to another range of time and stress and assume no change in failure mechanism.

The first method was considered here (Table IV-5). The exponential distribution is generally assumed when reliability is specified by a constant failure rate per 1000 hours (failure rates generally change with time, and other distributions, such as Weibull, log-normal, and Gamma are used in these cases). As previously noted, the cost and time involved in such a reliability demonstration is prohibitive. Therefore, the second method using short-term accelerated tests was adopted. The details of this matrix are discussed below.

3. Accelerated Test Matrix

Preliminary accelerated testing of HRLC product used both constant-stress and step-stress techniques. In principle, these procedures are essential to the determination of whether mechanisms occurring at high temperature are also activated at lower temperatures even if the constant stress techniques do not produce the failure at the lower temperature. In other words, the median time of the constant stress and median stress of the step stress should not differ significantly, as shown in Fig. IV-12.

As a result of the tests conducted and data received in the early stages of Phase II, it was decided to encapsulate HRLC devices with the silicone

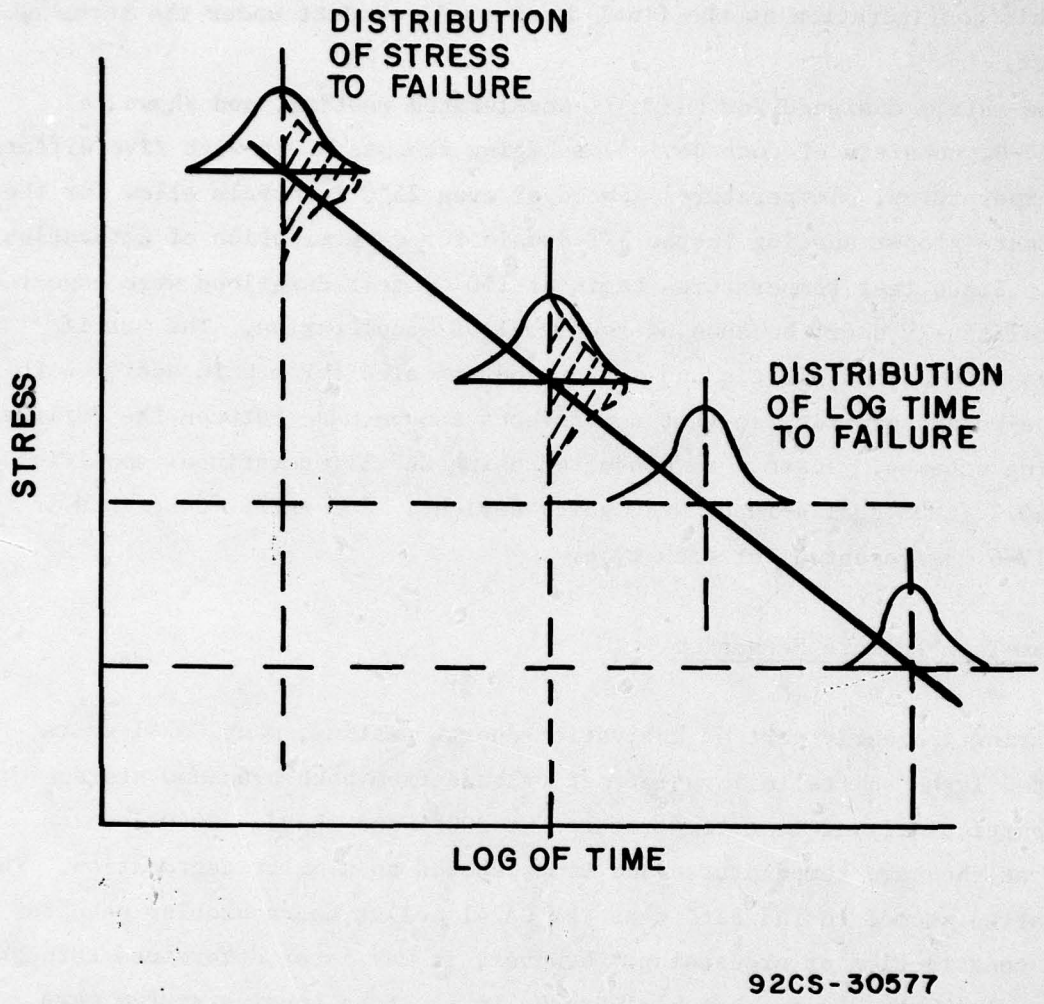

Fig. IV-12 - Step stress and constant stress relationship with time.

molding compound and to use these along with other control devices to generate activation-energy data for HRLC product. It was also decided to use devices with this configuration as the final deliverable product under the terms of the contract.

The matrix designed for Phase II accelerated testing, and shown in Table IV-6, consists of four device-packaging schemes along with five different test temperatures. Temperatures spaced at even 25°C intervals allow for the approximate proper spacing in the 1/T domain for determination of activation energy. Since test temperatures begin at 150°C, test durations were expected to be relatively short because of the level of acceleration. The matrix includes wire-bonded plastic and sealed and unsealed ceramic in addition to the tape-bonded plastic, so that comparisons can be made between the various packaging schemes. Tests were conducted using CA741 (operational amplifier) and CD4012 (CMOS dual 4-input NAND gate) devices. The matrix described in Table IV-6 was repeated for each type.

4. Beam-Tape Failure Mechanism

During the early part of activation-energy testing, many CA741 units exhibited large shifts in input-offset voltage from both bias and storage life, particularly at test temperatures of 200°C and above. CD4012 units tested at the same temperatures and times showed no similar degradation. This information seemed to indicate that the CA741 pellet had a problem peculiar to its construction or processing. However, it was later determined through additional thermal tests that heel breaks in the tape bonding system were occurring as a result of the limited thermal cycling resulting from down-period readings, and that these heel breaks caused high (and nonuniform) resistance in series with the corresponding input pin(s). The high resistance affected input-offset voltage measurements of the CA741, but did not initially affect measurements made on CD4012 COS/MOS units because of the nature of the circuit and electrical testing.

Table IV-6 - Matrix for Activation Energy Determination

CD4012 and CA741

	250°C	225°C	200°C	175°C	150°C	250°C	225°C	200°C	175°C	150°C
Tape Bonded Plastic	30	30	30	30	30	30	30	30	30	30
Wire Bonded Plastic	30	30	30	30	30	30	30	30	30	30
Sealed Ceramic	30	30	30	30	30	30	30	30	30	30
Unsealed Ceramic	30	30	30	30	30	30	30	30	30	30
	←- - - - - -Bias Life- - - - - -→					←- - - - -Storage Life- - - - - -→				

Down periods for 250°C bias and storage-life tests were specified at 2, 4, 8, 16, 32, 64, 128 and 256 hours. After four hours of high-temperature life (two down periods) several CA741 units were out of specification for input-offset voltage after storage and bias life. At 32 hours, the number of units out of specification for the same reason was 26% for combined storage and bias life. In the same 32-hour stress period, the CD4012 250°C tests produced three out-of-specification units for unrelated reasons. Later analysis revealed that the CD4012 units were exhibiting the same mechanisms as were the CA741 units. However, hot testing was required to make these mechanisms electrically evident.

On subjecting Phase II CA741 devices to thermal-shock tests, the same input-offset voltage drift was detected. After 100 cycles of liquid-to-liquid thermal shock, approximately 90% of the devices tested failed, primarily because of shifts in input-offset voltage. Normal 25°C testing revealed few open-circuited pins, but testing for continuity at elevated temperature showed many units open-circuited, mainly on the central pins on each side of the package (i.e., pins 3, 4, 5 and 10, 11, 12 on a 14-pin DIP). The decapping of thermal-shocked devices that failed hot-continuity testing revealed beam-tape heel cracks at the device bonding pad. The cracks were such that only high-resistance paths developed at 25°C but electrical open circuits occurred at 100°C ambient. Fig. IV-13 shows curve-tracer photos of input-continuity tests for a CA741 after 128 hours of 250°C storage life. The "on" portion of the slope of the unit in Fig. IV-13(b) indicates the increase in input resistance resulting from the fracture at the heel of the bond. The measurements were taken at pin 4, which is the inverting input to the unit.

5. Thermal-Shock Program to Improve HRLC System

The cross-sectional view in Fig. IV-14 shows the beam-tape finger, the inner-lead bond, and the bumped chip in the area where electrical testing indicated a high-resistance connection. The fracture in the beam tape is seen to occur at the heel of the inner-lead bond in the 0.003-inch width part of the beam (Fig. IV-15) which extends 15 to 20 mils from the end of the

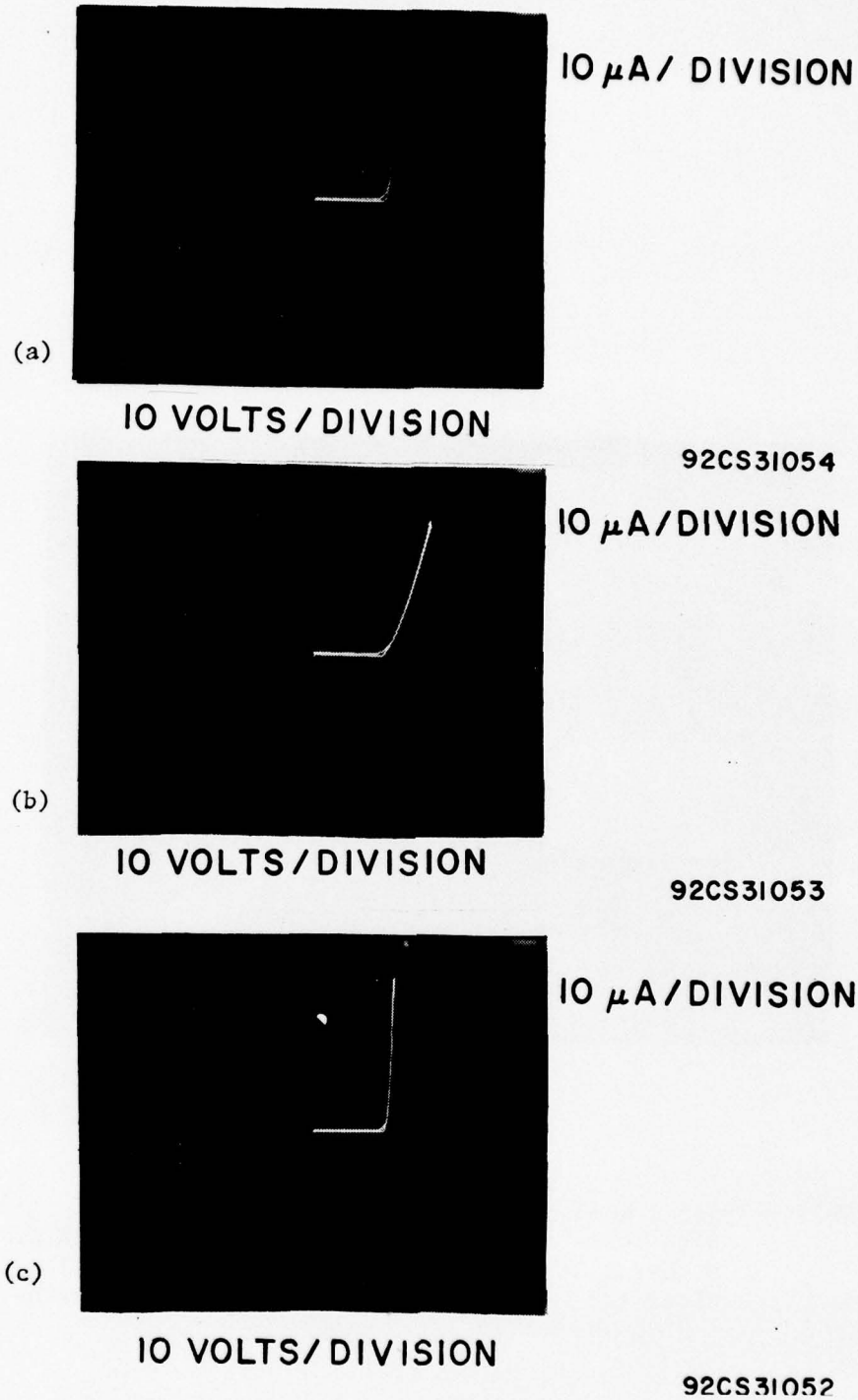

Fig. IV-13 - Typical curve-tracer examination of input resistance in CA741. (a) Control measurement. Good DIC, slope ≈ 60Ωk . (b) HRLC device on 250°C 128-hour storage-life test. Slope ≈ 330Ωk . Unit failed input-offset voltage test. (V_{IO} > 17 mV) (c) Same HRLC device as in (b) on 250°C 128-hour storage-life test after curve-tracer stress to close resistive gap. Slope ≈ 60Ωk . Unit now passes input-offset voltage test. (V_{IO} < 1 mV).

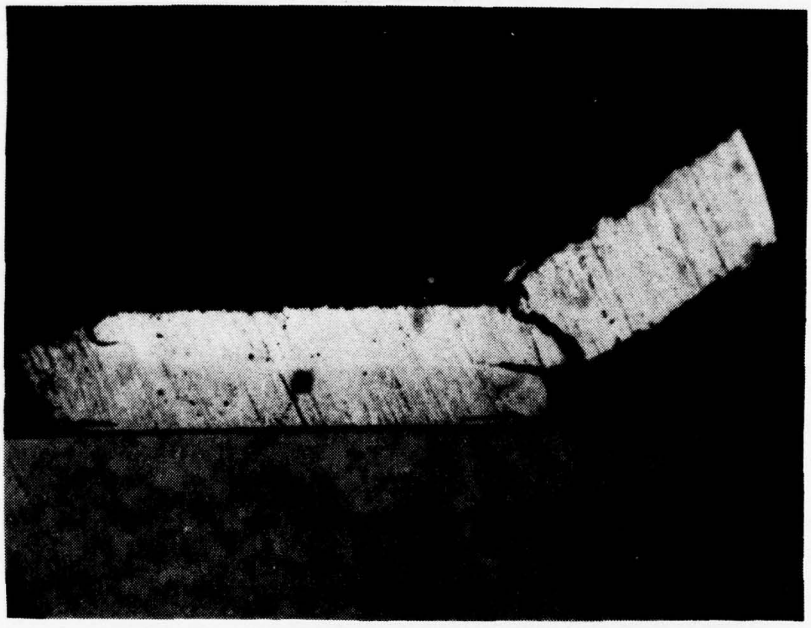

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Fig. IV-14 - Typical heel break.
High resistance = 200 k break of pin 11 on CA741 stressed at 250°C standard life. Device failed after 128 hours and 7 down periods. (V_{IO} = 17 mV)

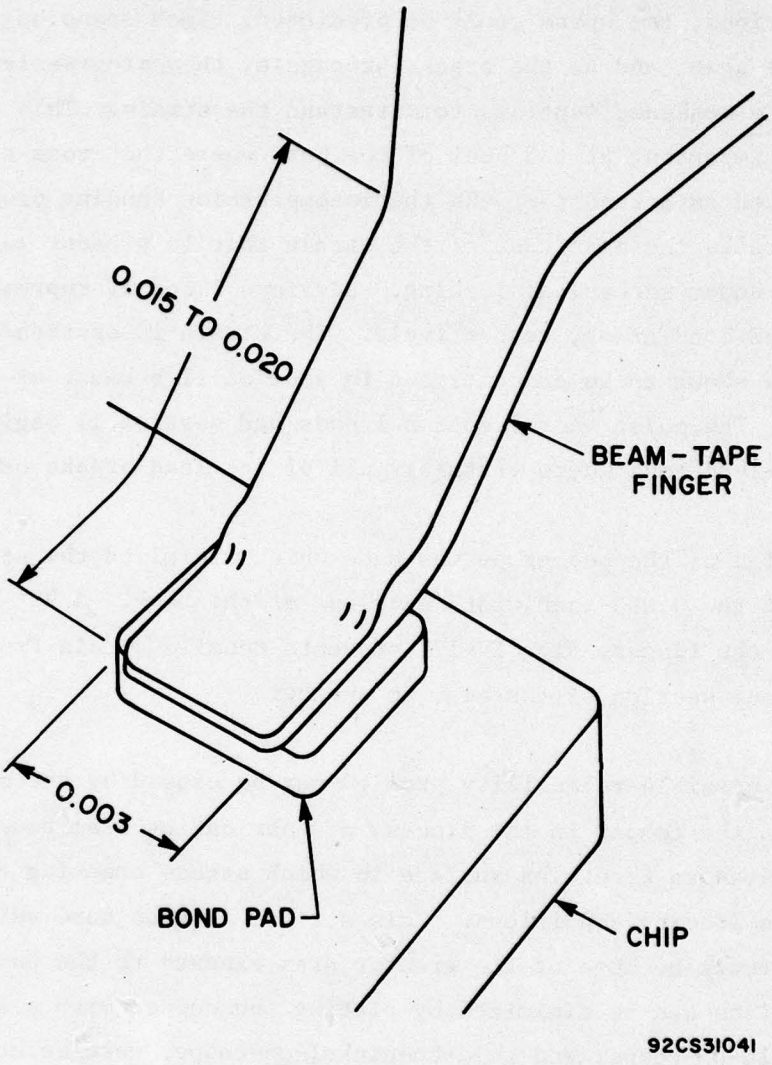

Fig. IV-15 - Schematic drawing of the portions of the beam-tape finger, inner-lead bond, and bumped chip involved in heel breaks.

finger. A study of the tape design revealed that, in this localized area, the total stress on the beam-tape finger is concentrated and that, under fatigue stress conditions, the opens could be predicted. Such opens begin as small cracks in the beam, and as the cracks propagate, they progressively reduce the ability of the weakened sections to withstand the strain. This condition is particularly important at the heel of the bond where the cross section of the lead is reduced as a result of the thermocompression bonding process. Fig. IV-16 illustrates the magnitude of the strain that is present in a straight, short finger under mechanical loading. Sections I and IV represent the inner and outer-lead bond areas, respectively. The strain in sections I and III under load is shown to be concentrated in section II because of the higher unit stress. The point where section I ends and section II begins is the heel of the inner-lead bond where virtually all of the lead breaks occur.

A redesign of the beam-tape was made which minimized the stress concentration in the 0.003-inch width sections of the tape. A 90° bend in the plan view of the finger, Fig. IV-17, prevents tensile strain from being transferred from one section of the beam to another.

Another possible reliability problem may be caused by the mild etchant used to clean the copper in the process of fabricating beam tape. This operation leaves an irregular surface in which stress cracking can originate during severe loading conditions. This surface is also more vulnerable to oxidation defects because of the greater area exposed to the environment. These conditions can be minimized by plating the copper with a suitable material; gold-on-copper and gold-on-nickel-on-copper were selected as the metallurgical systems to be evaluated.

A matrix of tests was devised to aid in an evaluation of the variables that affect the strength of the beam-tape system. The tests were arranged in cells of twenty units each; thermal-shock testing was selected as the method of exercising the assembled devices.

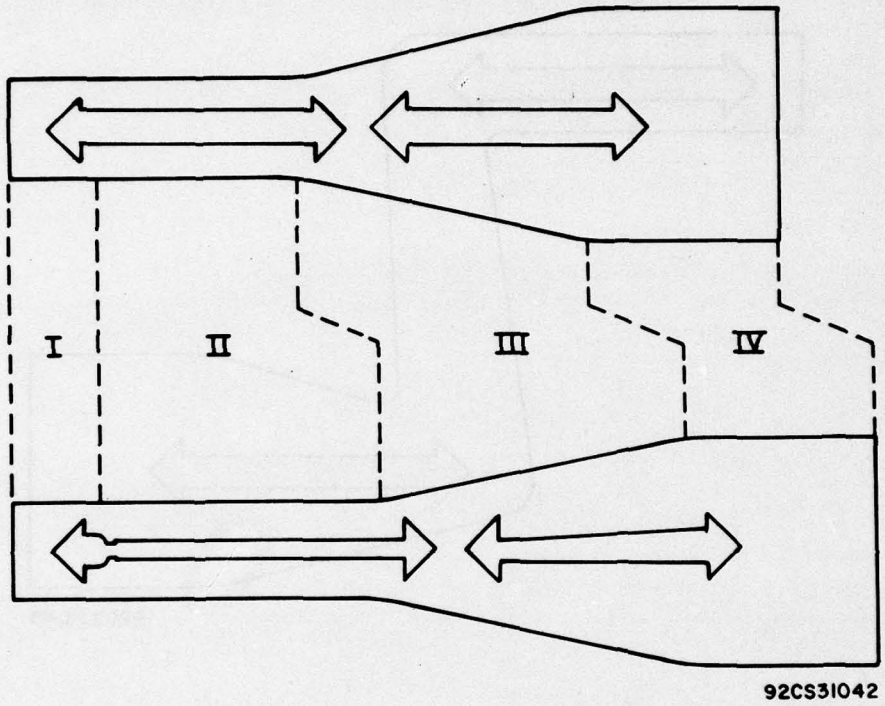

Fig. IV-16 - Strain in beam-tape finger.

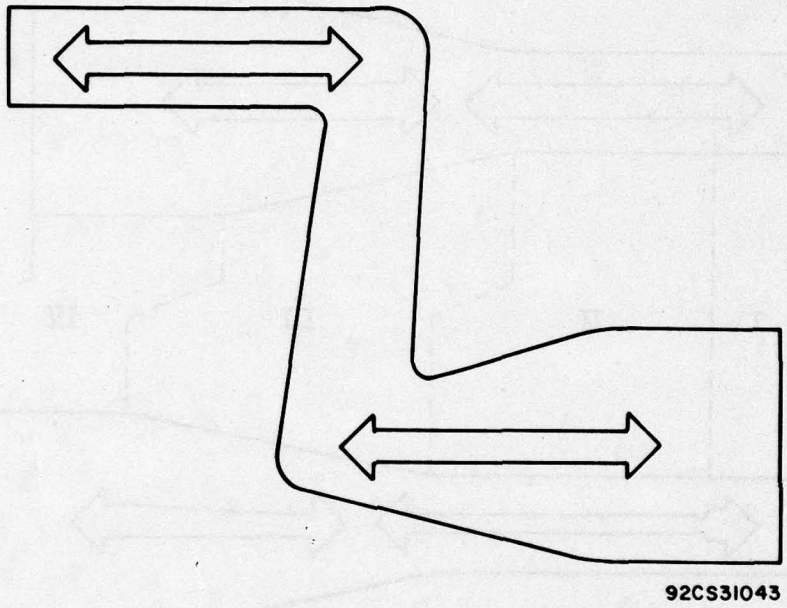

Fig. IV-17 - Strain in redesigned beam-tape finger.

Variables selected for comparison included:

1. Stress relief vs. no stress relief in the beam-tape design.
2. Copper beam-tape vs. gold-plated copper beam-tape vs. gold-plated nickel-plated copper beam tape.
3. Polyimide supported tape vs. unsupported tape.
4. Vendor A copper vs. Vendor B copper.
5. Silver-plated copper lead frames vs. spot gold-plated steel lead frames.

The test results are shown in Table IV-7. The most significant factors in the reliability performance of the cells tested were the stress-relief pattern and the plating on the beam-tape copper. There was no conclusive evidence that the presence of polyimide was a factor, nor was there any significant difference in the use of the copper from Vendor A over Vendor B. The lead frames performed identically and proved not to be a factor.

The results of the matrix tests clearly indicate that the stress-relief pattern is essential to the reliability of HRLC devices made with copper beam tape. Similarly, gold plating, with or without nickel plating, improved system resistance to thermal shock. Where most units made without stress-relief and gold-plated beam tape opened at less than 400 cycles of thermal shock (-65° to +150°C), devices with these features exhibited no problems after 2000 cycles.

E. Data Analysis

1. Composite Data Summary

A composite summary of the Phase II accelerated-life test results is presented in Tables IV-8 and IV-9. The number of MIL-STD-38510 limit failures are shown for each type in the upper left-hand corner of each cell square and the number of commercial data sheet limit failures are shown in the bottom right-hand corner. The starting sample for each test cell was 30 devices. Bias life on the HRLC samples was extended past the test time originally planned for

Table IV-7 - Thermal Shock -65°C to +150°C

Results: # Failures/ Sample Size

Device / Test No.	Beam Tape	Stress Relief	Polyimide	Au Plate	Ni-Au Plate	Cu Lead Frame	Fe Lead Frame	Silicone Compound	100 Cycles	500 Cycles	1000 Cycles	1500 Cycles	2000 Cycles
CA741 02	VENDOR "A"		X			X		X	29/29				
E19	VENDOR "A"				X		X	X		20/20			
E20	VENDOR "A"		X		X		X	X		20/20			
E21	VENDOR "A"		X				X	X		20/20			
E22	VENDOR "A"	X			X		X	X		0/20	0/20	0/20	0/20
E23	VENDOR "B"	X					X	X		0/20	8/20		
E26	VENDOR "B"	X			X	X		X		0/20	0/20	1/20	
E27	VENDOR "B"	X				X		X		1/20	8/19		
E29	VENDOR "B"	X				X		X		7/20			
E30	VENDOR "B"	X		X		X		X		0/20	0/20	0/20	1/20
E31	VENDOR "B"	X			X	X		X		0/20	0/20	0/20	3/20
E32	VENDOR "B"	X			X		X	X		0/20	0/20	0/20	3/20

Table IV-7 (Continued)

Failures/Sample Size

Results:

Devices / Test No.		Beam Tape	Stress Relief	Polyimide	Au Plate	Ni-Au Plate	Cu Lead Frame	Fe Lead Frame	Silicone Compound	100 Cycles	500 Cycles	1000 Cycles	1500 Cycles	2000 Cycles
CA741	E12	VENDOR "B"						X	X	1/20	3/19			
	E13	VENDOR "A"	X		X			X	X		0/14	0/14	0/14	
	E15	VENDOR "A"	X					X	X		0/16	0/16	2/16	0/14
	E20	VENDOR "A"		X		X		X	X	0/20	0/20	20/20		
	E21	VENDOR "A"	X			X		X	X		0/20		0/20	
	E22	VENDOR "A"	X	X		X		X	X		6/20			
	E23	VENDOR "A"		X	X			X	X		4/20			

Table IV-8 - Phase II Matrix, CA741

CA741

	Bias Life						Storage Life			
	250°C, 256 Hr.	225°C, 256 Hr.	200°C, 256 Hr.	175°C, 1,344 Hr.	150°C, 1,500 Hr.	250°C, 256 Hr.	225°C, 256 Hr.	200°C, 256 Hr.	175°C, 1,344 Hr.	150°C, 2,000 Hr.
HRLC	26 10	2 1	4 3	0 0	0 0	3 1	0 0	1 1	0 0	1 0
PLASTIC W.B.	20 4	3 0	2 0	1 1	2 1	1 0	2 1	1 1	1 0	0 0
DIC SEALED	18 1	1 1	4 1	1 1	1 0	0 0	2 2	0 0	2 1	2 0
DIC UNSEALED	21 3	1 0	2 0	1 0	1 0	0 0	0 0	1 0	0 0	1 0
HRLC (Extended Time)	27 A 17	2 B 1	4 C 3	0 D 0	0 E 0					

Key: Mil / Comml

A=1,500 Hrs.
B=1,500 Hrs.
C= 992 Hrs.
D=2,000 Hrs.
E=2,000 Hrs.

Sample Size: N=30

Electrical Test Criteria

Measurement	CA741 MIL Limit	Commercial Limit
VIO	± 3 mV max.	± 5 mV max.
IIB	± 1.0 nA to ± 110 nA	± 380 nA max.
IIO	± 30 nA max.	± 200 nA max.
CMR	80 dB min.	70 dB min.
IOS	± 60 mA max.	± 60 mA max.
ICC	3.8 mA max.	2.8 mA max.
AOL	50 min. V/mV	50 min. V/mV
PSRR	100 µV/V max.	150 µV/V max.

Table IV-9 - Phase II Matrix, CD4012

CD4012

	BIAS LIFE						STORAGE LIFE			
	250°C, 256 Hr.	225°C 256 Hr.	200°C, 256 HR.	175°C, 1,344 Hr.	150°C, 1,500 Hr.	250°C, 256 Hr.	225°C, 256 Hr.	200°C, 256 Hr.	175°C, 1,344 Hr.	150°C, 2,000 Hr.
HRLC	16 6	16 2	14 2	4 1	7 0	1 0	0 0	1 0	3 0	0 0
PLASTIC W.B.	10 2	9 2	9 3	6 1	5 2	1 0	4 1	5 0	2 0	2 2
DIC SEALED	9 2	6 3	6 1	4 2	19 2	8 1	4 1	5 0	30 0	30 0
DIC UNSEALED	23 6	23 3	4 3	9 1	10 4	21 1	19 0	14 1	24 1	26 1
HRLC (EXTENDED TIME)	21 A 6	18 B 2	17 C 7	5 D 1	1 E 0					

A=1,048 Hrs.
B=1,500 Hrs.
C=1,336 Hrs.
D=2,000 Hrs.
E=1,836 Hrs.

Electrical Test Criteria

CD4012

Measurement	Mil Limit	Commercial Limit
ISS	25 nA max.	1μA max.
VOH loaded	4.2V min.	N/A
VOH unloaded	4.95V min.	4.95V min.
VOL loaded	.7V max.	N/A
VOL unloaded	.95V max.	.95V max.
IIH	1 nA max.	100 nA max.
IIL	1 nA max.	100 nA max.

Phase II; these results are shown at the bottom of the matrix for each type. The results of this matrix of tests will be discussed in detail by device type starting with the CA741 in the paragraphs that follow.

2. Electrical Test Criteria

Listings of the electrical parameters measured and corresponding limits criticized in the evaluation are also shown in Tables IV-8 and IV-9.

3. CA741-Bias-Life Results

A detailed summary listing the results of the four package versions by down time (noncumulative) is shown in Tables IV-10, IV-11, IV-12, and IV-13. Units were not removed from test unless they failed the commercial limits. The total number of failures for each test is shown at the bottom of each Table. MIL-STD failures were primarily for I_{IB}; commercial failures were primarily for V_{IO}.

An examination of these tables shows that the majority of failures (particularly for the MIL-STD limits) occurred at 250°C, with very few failures exhibited at the lower temperatures. This situation becomes more evident from the plots showing the total percentage of failures in Figs. IV-18 and IV-19 (the plots exclude the extended time for HRLC). A determination of the failure distributions for the temperatures below 250°C was not possible because of the small number of failures experienced within the designated Phase II test durations. At 250°C the "desired" high percentage of MIL-STD failures occurred. However, these tended to cluster at one particular down time within each of the package versions, so that the data could not be adequately fitted to a log-normal failure distribution. Most of the MIL-STD failures exceeded the I_{IB} limit of 110 nA by a small amount (approximately 10 to 20 nA). Additional test time showed little or no further degradation in I_{IB} for these same units, so that a degradation trend in I_{IB} was not clearly evident.

RCA

Table IV-10

NAVELEX DATA SUMMARY - PHASE II

Type and Description CA741 Auto Dip (HRLC) Test Bias Life 30V

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=28)			225°C (N= 29)			200°C (N= 30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	0	0	2	0	0	2	3	3	8	0	0	8	0	0
4	0	0	4	0	0	4	0	0	24	0	0	24	0	0
8	0	0	8	1	0	8	0	0	168	0	0	168	0	0
16	0	0	16	0	0	16	0	0	336	0	0	500	0	0
32	4	3	32	0	0	32	0	0	672	0	0	1000	0	0
64	3	1	64	0	0	64	0	0	1000	0	0	1500	0	0
128	6	3	128	0	0	128	0	0	2000	0	0	2000	0	0
256	13	3	256	1	1	256	1	0						
512	0	3	424	0	0	512	0	0						
1500	1	4	1500	0	0	992	0	0						
Total	27	17	/	2	1	/	4	3	/	0	0	/	0	0

RCA

Table IV-11

NAVELEX DATA SUMMARY - PHASE II

Type and Description CA741 DIP Wire Bonded Test Bias Life 30V

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	0	0	2	0	0	2	0	0	8	1	1	8	1	0
4	0	0	4	0	0	4	0	0	24	0	0	24	0	0
8	1	1	8	1	0	8	1	0	168	0	0	168	0	0
16	13	2	16	0	0	16	0	0	336	0	0	500	0	0
32	2	0	32	0	0	32	1	0	672	0	0	1000	0	0
64	0	0	64	1	0	64	0	0	1008	0	0	1500	1	1
128	4	1	128	1	0	128	0	0	1344	0	0			
256	0	0	256	0	0	256	0	0						
Total	20	4		3	0		2	0		1	1		2	1

RCA

Table IV-12

NAVELEX DATA SUMMARY - PHASE II

Type and Description CA741 DIC Wire Bonded Test Bias Life 30V

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N= 30)			225°C (N=29)			200°C (N=30)			175°C (N=30)			150°C (N= 30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	1	1	2	0	0	2	0	0	8	0	0	8	0	0
4	1	0	4	0	0	4	0	0	24	0	0	24	0	0
8	1	0	8	0	0	8	0	0	168	0	0	168	0	0
16	1	0	16	1	1	16	0	0	336	0	0	500	1	0
32	10	0	32	0	0	32	0	0	672	0	0	1000	0	0
64	0	0	64	0	0	64	0	0	1000	1	1	1500	0	0
128	3	0	128	0	0	128	4	1	1344	0	0			
256	1	0	256	0	0	256	0	0						
Total	18	1	/	1	1	/	4	1	/	1	1	/	1	0

RCA

Table IV-13

NAVELEX DATA SUMMARY - PHASE II

Type and Description CA741 DIC (Unsealed) Wire Bonded Test Bias Life 30V

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	0	0	2	0	0	2	0	0	8	1	1	8	0	0
4	1	0	4	0	0	4	0	0	24	0	0	24	0	0
8	4	0	8	0	0	8	2	0	168	0	0	168	1	0
16	0	0	16	1	0	16	0	0	336	0	0	500	0	0
32	13	3	32	0	0	32	0	0	672	0	0	1000	0	0
64	0	0	64	0	0	64	0	0	1000	0	0	1500	0	0
128	1	0	128	0	0	128	0	0	1344	0	0			
256	2	0	256	0	0	256	0	0						
Total	21	3	/	1	0	/	2	0	/	1	1	/	1	0

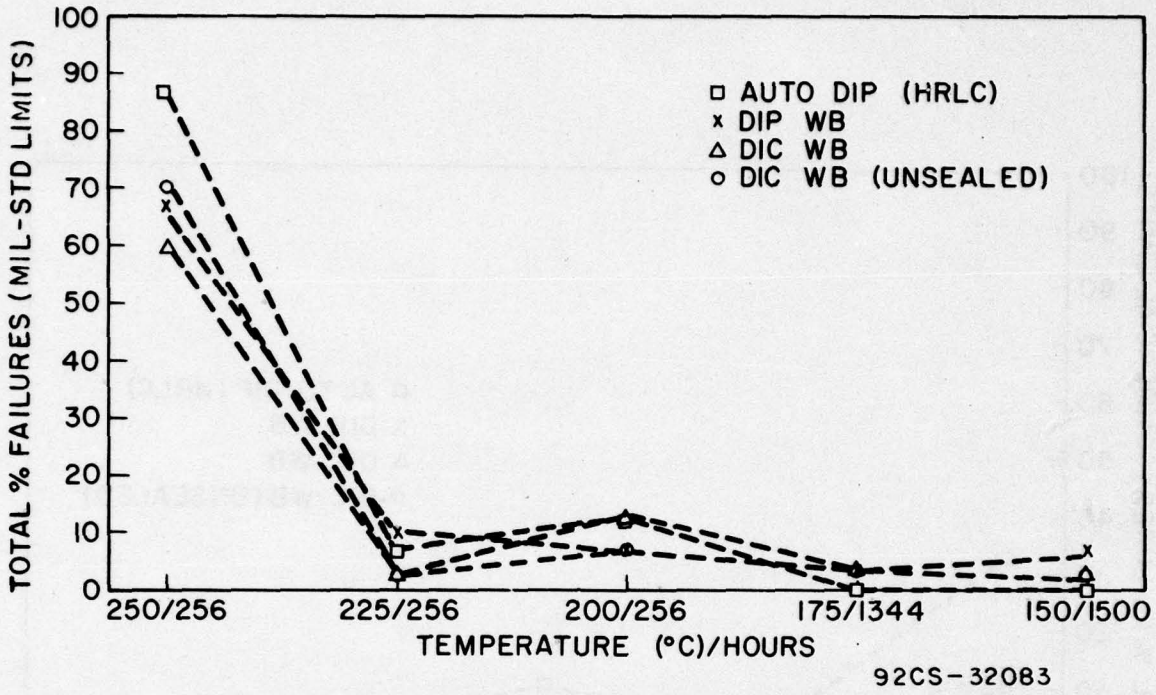

Fig. IV-18 - CA741 bias life, comparison of package systems for total percent failures relative to temperature (MIL-STD limits).

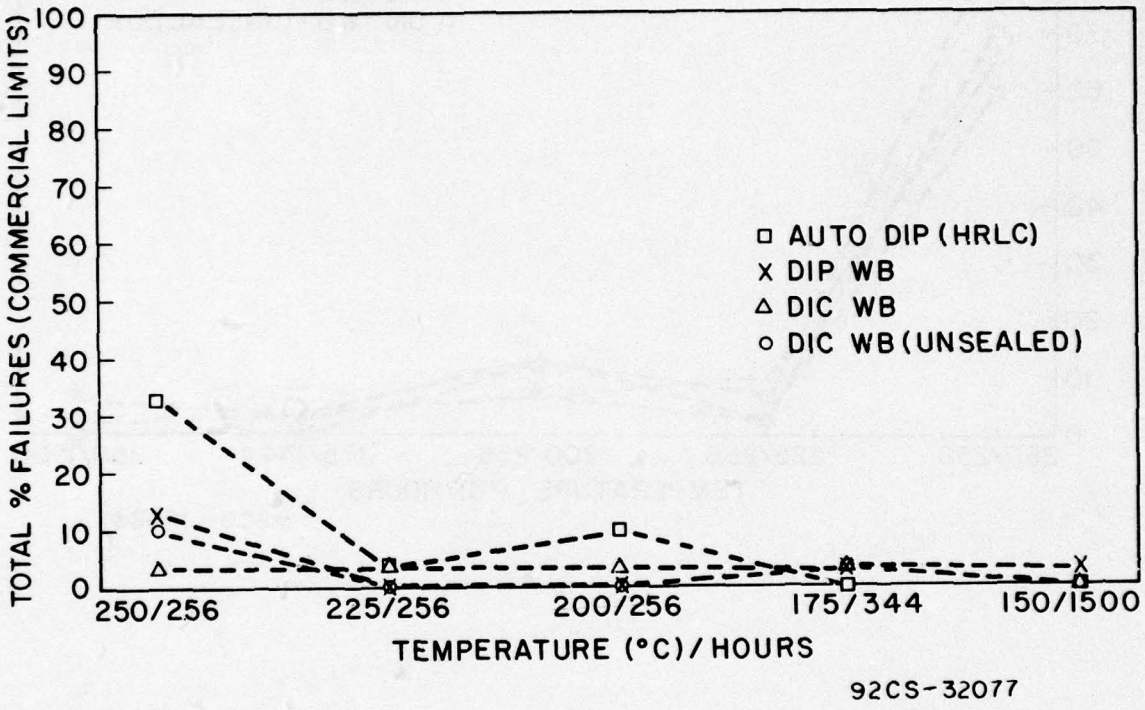

Fig. IV-19 - CA741 bias life; comparison of package system for total percent failures relative to temperature (commercial limits).

All of the tests in the HRLC group were extended past the Phase II designated time durations in order to produce a sufficient number of failures to determine failure distributions, particularly for the temperatures below 250°C commercial limits. The results for the test times completed as of this writing are shown in Table IV-10. For the temperatures below 250°C no additional failures occurred for either MIL-STD or commercial limits. However, additional commercial limit failures (primarily V_{IO}) were experienced at 250°C. These failures were fitted to a log-normal distribution, having a sigma value of 2.6 and a Median-Time-to-Failure (MTF) of about 750 hours (Fig. IV-20), however, the analysis of these devices (see pages IV-85-86) concluded that the failure mode was beam lifts caused by marginal beam-to-chip bond contact. This anomalous failure mode invalidates the 250°C data from the standpoint of being used for estimating the HRLC activation energy and failure rate. Because of this fact and the fact that too few failures have occurred below 250°C, no HRLC failure rate estimate can be made at this time.

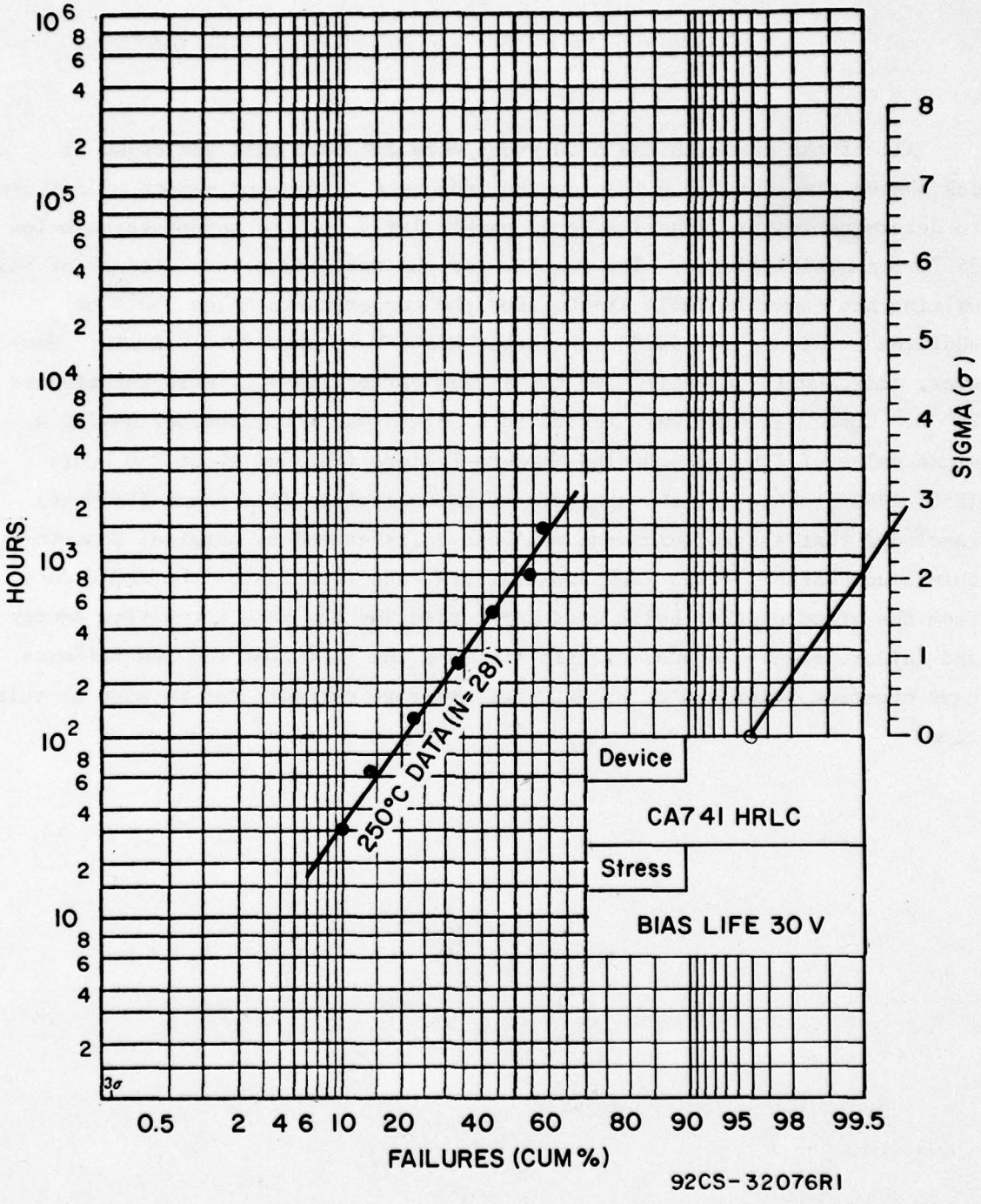

Fig. IV-20 - CA741 HRLC bias life, 30V; commercial electrical limits.

4. CA741 - Storage Life Results

The data for storage life is shown in Tables IV-14, IV-15, IV-16, and IV-17. A review of these tables shows that very few limit failures have occurred with no significant trends established. The significant difference in results between the storage life data and the bias life data at 250°C shows that the effects of the bias voltage were not cancelled out by the high-temperature stress.

5. CA741 - Comparison of Package Systems

A direct comparison of the HRLC system with the other package variations is not straightfoward from the standpoint that the measures taken to correct the beam-tape configuration (described previously) necessitated using, in the resubmitted samples, pellets from a different wafer lot than those used in the other package systems. Analysis of the individual wafer results showed a high degree of variability. Fig. IV-21 shows a plot of the wafer variability within each package system, as evidenced at 250°C after 256 hours of bias life (MIL-STD limits). The HRLC group consisted of only one wafer, which exhibited 86% failures, while the other package variations shared four different wafers, which exhibited a range of 20-100% failures. This plot shows that the HRLC wafer results are within the range of variability of the four wafers used in the other package systems.

A plot of the combined test results for each package system is shown in Fig. IV-22 (the figure excludes the extended HRLC time). Application of the Chi-Square test showed no significant difference $[\chi^2(3, .01)]^{(1)}$ among the four package systems with regard to storage life (MIL-STD and commercial limits) and bias life (MIL-STD limits). The bias life for commercial limits was marginally significant, however, this is probably attributable to the wafer effect described above.

6. CD4012 - Bias Life Results

A detailed tabulation of the data by downtime is shown in Tables IV-18, IV-19, IV-20, and IV-21. A plot of the percentage of limit failures obtained for each package system at the completion of the Phase II time

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Table IV-14

NAVELEX DATA SUMMARY - PHASE II

Type and Description: CA741 Auto Dip (HRLC) Test: Storage Life

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time

250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	0	0	2	0	0	2	0	0	8	0	0	8	0	0
4	1	0	4	0	0	4	0	0	24	0	0	24	0	0
8	0	0	8	0	0	8	0	0	168	0	0	168	0	0
16	0	0	16	0	0	16	0	0	336	0	0	500	0	0
32	0	0	32	0	0	32	1	1	672	0	0	1000	0	0
64	1	1	64	0	0	64	0	0	1000	0	0	1500	1	0
128	1	0	128	0	0	128	0	0	1344	0	0			
256	0	0	256	0	0	256	0	0	2000	0	0			
Total	3	1	/	0	0	/	1	1	/	0	0	/	1	0

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TAble IV-15

NAVELEX DATA SUMMARY - PHASE II

Type and Description CA741 DIP Wire Bonded Test Storage Life

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N= 30)			225°C (N=30)			200°C (N= 30)			175°C (N= 30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	0	0	2	0	0	2	1	1	8	0	0	8	0	0
4	1	0	4	1	0	4	0	0	24	1	0	24	0	0
8	0	0	8	0	0	8	0	0	168	0	0	168	0	0
16	0	0	16	0	0	16	0	0	336	0	0	500	0	0
32	0	0	32	1	1	32	0	0	672	0	0	1000	0	0
64	0	0	64	0	0	64	0	0	1344	0	0	1500	0	0
128	0	0	128	0	0	128	0	0				2000	0	0
256	0	0	256	0	0	256	0	0						
Total	1	0		2	1		1	1		1	0		0	0

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Table IV-16

NAVELEX DATA SUMMARY - PHASE II

Type and Description: CA741 DIC Wire Bonded Test: Storage Life

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	0	0	2	1	1	2	0	0	8	0	0	8	0	0
4	0	0	4	0	0	4	0	0	24	1	0	24	0	0
8	0	0	8	0	0	8	0	0	168	0	0	168	0	0
16	0	0	16	0	0	16	0	0	336	0	0	500	1	0
32	0	0	32	0	0	32	0	0	672	1	1	1000	0	0
64	0	0	64	0	0	64	0	0	1344	0	0	1500	1	0
128	0	0	128	0	0	128	0	0				2000	0	0
256	0	0	256	1	1	256	0	0						
Total	0	0	/	2	2	/	0	0	/	2	1	/	2	0

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Table IV-17

NAVELEX DATA SUMMARY - PHASE II

Type and Description CA741 DIC (Unsealed) Wire Bonded Test Storage Life

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	0	0	2	0	0	2	0	0	8	0	0	8	0	0
4	0	0	4	0	0	4	1	0	24	0	0	24	0	0
8	0	0	8	0	0	8	0	0	168	0	0	168	0	0
16	0	0	16	0	0	16	0	0	336	0	0	500	0	0
32	0	0	32	0	0	32	0	0	672	0	0	1000	0	0
64	0	0	64	0	0	64	0	0	1344	0	0	1500	1	0
128	0	0	128	0	0	128	0	0				2000	0	0
256	0	0	256	0	0	256	0	0						
Total	0	0	/	0	0	/	1	0	/	0	0	/	1	0

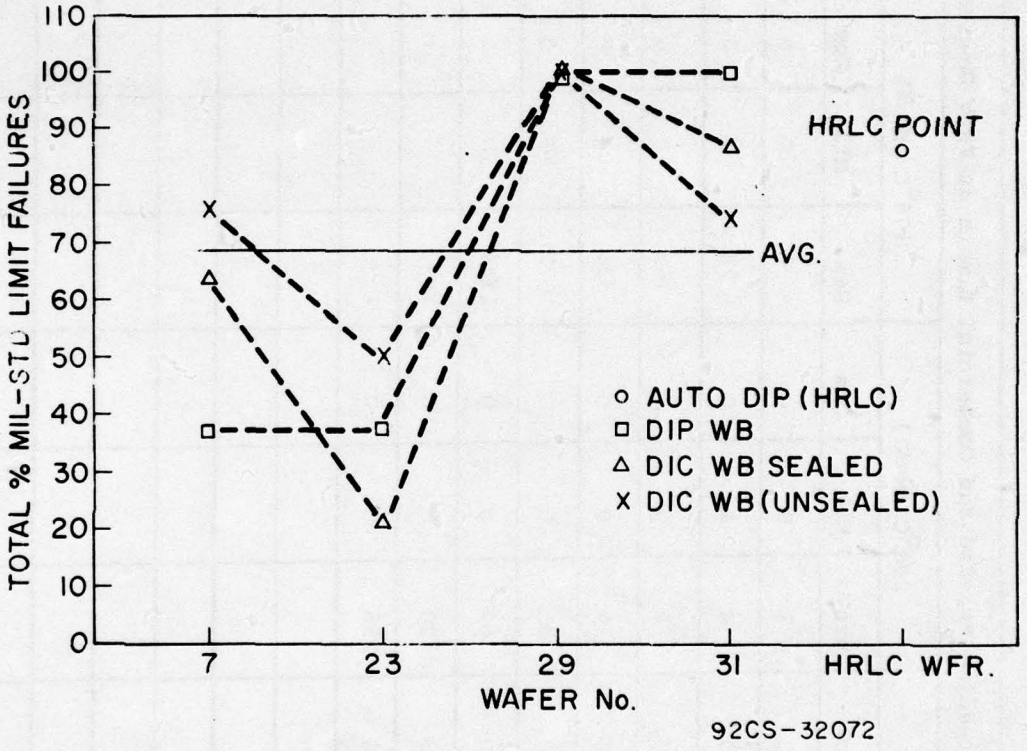

Fig. IV-21 - CA741 bias life, 30V, plot of wafer variability (MIL-STD limits).

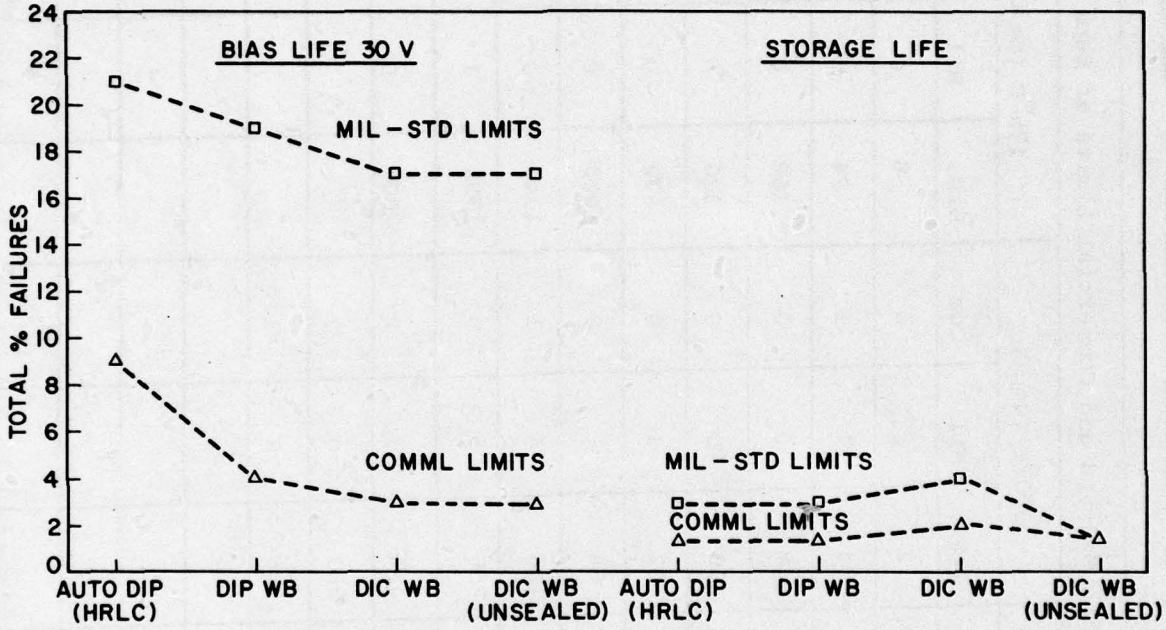

Fig. IV-22 - CA741 bias and storage life, comparison of package systems for total percent failures.

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Table IV-18

NAVELEX DATA SUMMARY - PHASE II

Type and Description CD4012 Auto Dip (HRLC) Test Bias Life 12.5V

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time

250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30) (a)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	1	0	2	3	0	2	2	0	8	4	1	8	2	0
4	1	0	4	2	1	4	1	1	24	0	0	24	2	0
8	1	0	8	0	0	8	0	0	168	0	0	168	2	0
16	4	0	16	1	0	16	0	0	336	0	0	500	1	0
32	2	1	32	3	1	32	1	0	672	0	0	1000	0	0
64	5	0	64	0	0	64	1	0	1000	0	0	1500	0	0
128	1	3	128	4	0	128	4	1	1344	0	0	1836	0	0
256	1	2	256	3	0	256	5	0	1680	1	0			
424	1	0	424	0	4	424	3	2	2000	0	0			
880	4	4	880	1	2	880	0	2						
1048	0	0	1500	1	1	1336	0	1						
Total	21	10		18	9		17	7		5	1		7	0

(a) 7 units removed: 3 broken pins, 4 VSS diode

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Table IV-19
NAVELEX DATA SUMMARY - PHASE II

Type and Description CD4012 DIP Wire Bonded Test Bias Life 12.5V

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	-	-	2	1	1	2	1	1	8	1	1	8	-	-
4	-	-	4	-	-	4	-	-	24	-	-	24	-	-
8	-	-	8	-	-	8	4	2	168	-	-	168	-	-
16	3	0	16	-	-	16	0	0	336	2	0	500	4	1
32	1	0	32	3	0	32	1	0	672	1	0	1000	1	1
64	5	1	64	2	0	64	1	0	1000	1	0	1500	0	0
128	1	1	128	3	1	128	1	0	1344	1	0			
256	0	0	256	0	0	256	1	0						
Total	10	2	/	9	2	/	9	3		6	1		5	2

RCA

Table IV-20

NAVELEX DATA SUMMARY - PHASE II

Type and Description CD4012 DIC Wire Bonded Test Bias Life 12.5V

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	-	-	2	-	-	2	-	-	8	0	0	8	-	-
4	-	-	4	-	-	4	-	-	24	0	0	24	-	-
8	-	-	8	-	-	8	3	1	168	1	1	168	1	1
16	5	0	16	1	1	16	1	0	336	2	0	500	4	0
32	3	1	32	1	1	32	0	0	672	1	0	1000	14	1
64	0	1	64	0	0	64	1	0	1000	0	0	1500	0	0
128	1	0	128	4	0	128	0	0	1344	0	1			
256	0	0	256	0	1	256	1	0						
Total	9	2	/	6	3	/	6	1	/	4	2	/	19	2

RCA

Table IV-21

NAVELEX DATA SUMMARY - PHASE II

Type and Description CD4012 DIC (Unsealed) Wire Bonded Test Bias Life 12.5V

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=28)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	-	-	2	-	-	2	-	-	8	-	-	8	-	-
4	-	-	4	-	-	4	-	-	24	-	-	24	-	-
8	-	-	8	-	-	8	2	-	168	-	-	168	-	-
16	5	1	16	-	-	16	0	0	336	1	1	500	1	1
32	1	3	32	3	1	32	0	0	672	4	0	1000	6	0
64	2	2	64	2	0	64	1	0	1000	1	0	1500	3	3
128	15	0	128	15	2	128	0	0	1344	3	0			
256	0	0	256	3	0	256	1	1						
Total	23	6		23	3		4	1		9	1		10	4

designations (excludes extended HRLC time) is shown in Figs. IV-23 and IV-24. An analysis of these results showed no significant temperature trends [$\chi^2(3, .01)$] in the range of 200°C to 250°C within each package system (except for the DIC unsealed system at 200°C). That is, for the same test duration of 256 hours these temperatures exhibited a similar percentage of failures (MIL-STD and commercial limits) so that a time-temperature relationship could not be established. This situation was also observed for the 175°C (1344 hours) and 150°C (1500 hours) temperatures.

At this point some comments are made concerning the MIL-STD limit failures. The majority of the MIL-STD failures at the time of failure exceeded the limits by a small amount. The primary indicators were I_{LL} at 1 nanoampere and I_{SS} at 25 nanoamperes. Typically these limits were exceeded by 1 to 10 nanoamperes. Most often the devices in this range recovered within limits by a succeeding downtime. On the other hand, units which degraded more than 200 nA above the limit continued to degrade on succeeding down times.

The commercial limit failures shown primarily exceeded the I_{SS} limit of 1 microampere. However, not enough commercial limit failures occurred within the designated Phase II time durations to obtain failure distributions. Thus, the test time in the HRLC group was extended; these results are shown in Table IV-18.

An analysis of the HRLC results showed a highly significant wafer effect. This wafer effect was observed in the other package systems as well, and is best demonstrated in Fig. IV-25 and Table IV-22. Fig. IV-25 is a plot of the MIL-STD failures relative to the wafers used in each package system for the combined test results (excludes extended HRLC time). The HRLC group used different wafer lots for reasons explained previously in the CA741 section

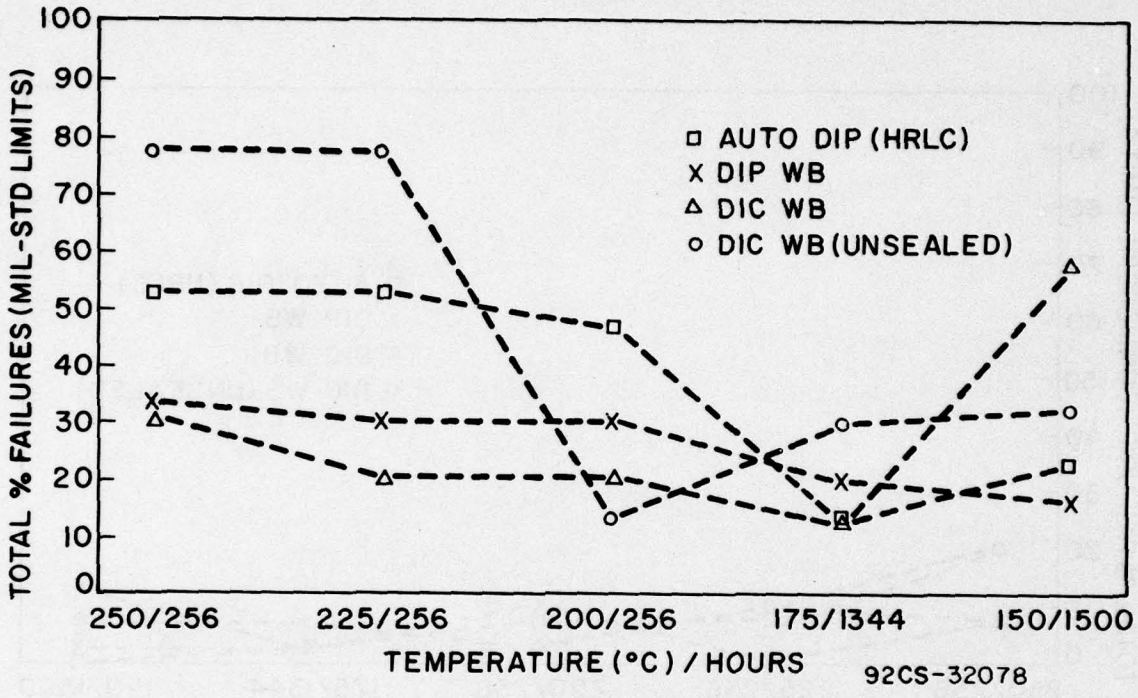

Fig. IV-23 - CD4012 bias life, comparison of package systems for total percent failures with temperature (MIL-STD limits).

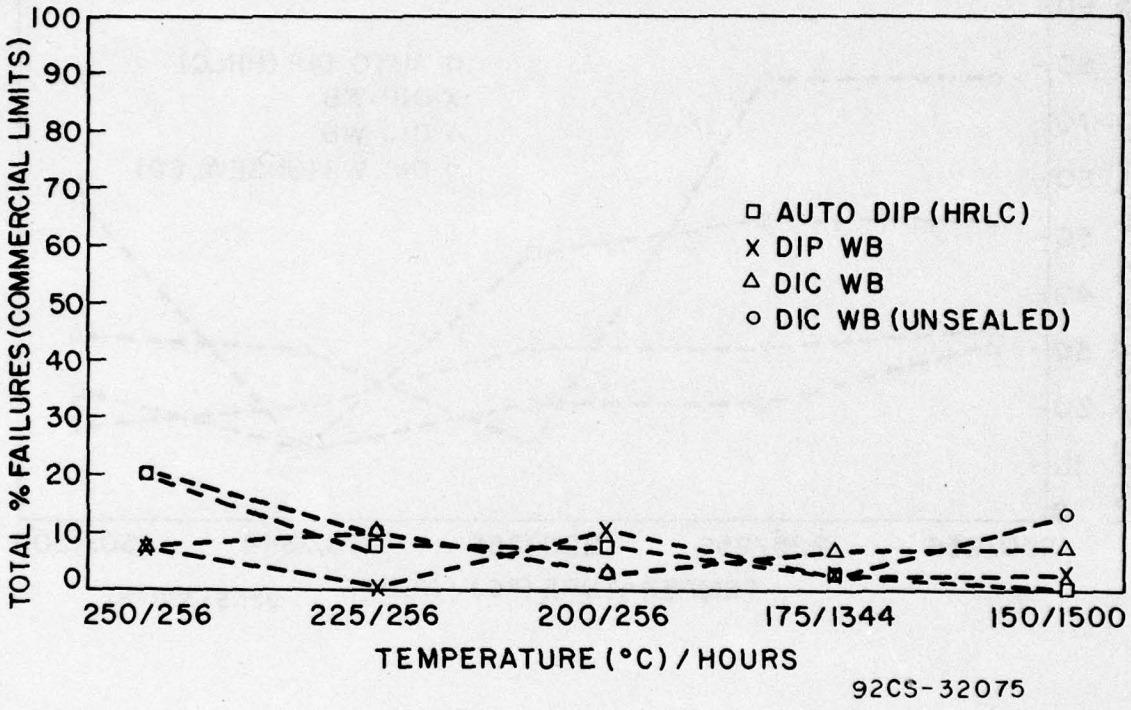

Fig. IV-24 - CD4012 bias life, comparison of package systems for total percent failures relative to temperature (commercial limits).

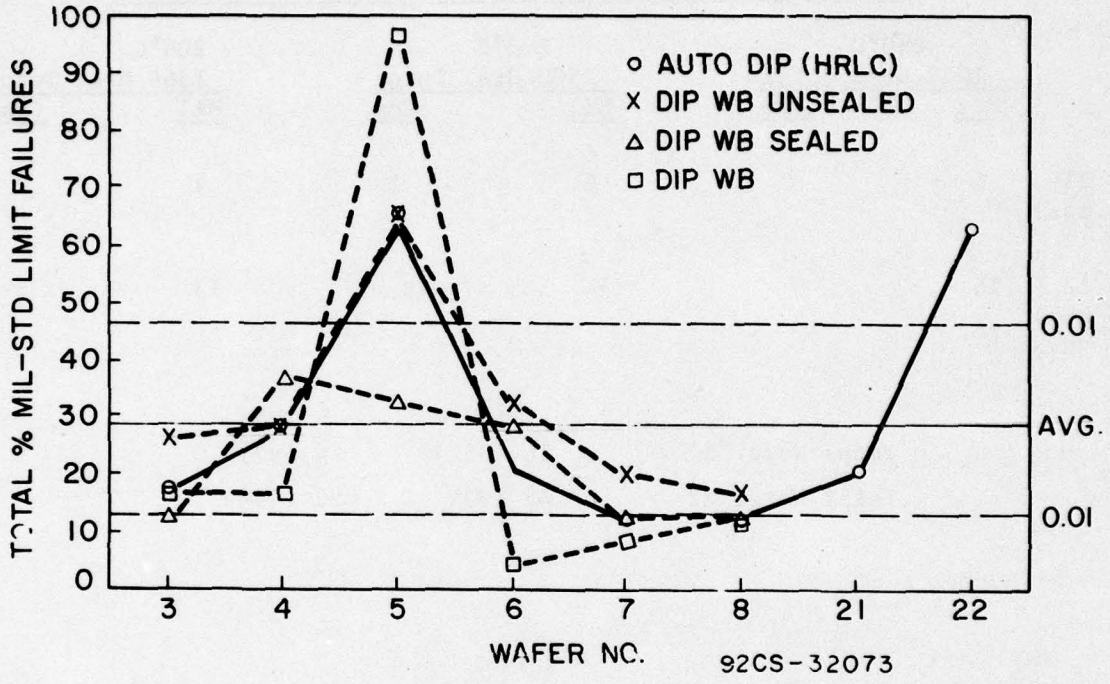

Fig. IV-25 - CD4012 bias life, 12.5V, plot of wafer variability; total percent MIL-STD limit failures for combined temperatures and test times.

Table IV-22 - CD4012 AUTODIP (HRLC)
Comparison of Wafers 21 and 22 on Bias Life

Number of Units Exceeding MIL-STD & Commercial Limits

	250°C 1048 Hrs. Total		225°C 1500 Hrs. Total		200°C 1366 Hrs. Total	
	Mil	Com	Mil	Com	Mil	Com
Wafer 21 (N=15 ea.)	6	1	6	1	4	2
Wafer 22 (N=15 ea.)	15	9	14	8	13	5

	Mil	Com
Total Wafer 21	16 (35%)	4 (9%)
Total Wafer 22	42 (93%)	22 (49%)

of this report. The points connected by the solid line in Fig. IV-25 represent the average wafer variability independent of the package, while the dashed lines represent the wafer-package variation. The decision lines (.01 level of significance) were computed from the Analysis of Means[2] as performed on the wafer results, independent of package (solid line). This computation showed both wafer 5 and wafer 22 to be significant (above the decision lines). Wafer 5 was influenced by the DIP package results, which showed failures for V_{OH} loaded (the only wafer to exhibit this). A separate analysis of this wafer will be presented later in this report. Wafer 22 in the HRLC group exhibited failures primarily for I_{LL} and I_{SS}, as previously discussed.

An additional analysis was performed on the HRLC wafers, 21 and 22, with respect to the extended test time at 200 to 250°C (see Table IV-22). Wafer 22 showed a significantly higher percentage of failures [$\chi^2(1, .01)$] for both MIL-STD and commercial limits than was experienced by wafer 21. Because of this difference, additional test time may show entirely different failure distributions, and possibly activation energies, for these two wafers. For this reason, wafer 22 was analyzed separately in terms of plotting the HRLC failure distributions. Wafer 21 did not experience enough failures to allow plotting of distributions.

The failure distributions of wafer 22 were determined by using a limit for $I_{SS} \geq 250$ nanoamperes. This limit was chosen because it provided the clearest distinction between temperatures. The distributions for the 200°C, 225°C, and 250°C temperatures are shown in Figs. IV-26 through IV-28. (The temperatures of 175°C and 150°C did not show enough failures to allow plots of distribution). An adjustment for early failures was made in Figs. IV-26 and IV-27.[3] As shown, the sigma values for the adjusted data varied between 1.5 and 2.2. However, Bartlett's test,[4] conducted on the variances, showed no significant difference [$\chi^2(2, .01)$] among these sigma values, based on the sample sizes tested. An Arrhenius plot made from the MTF values obtained from these distributions showed an activation energy of 0.55, Fig. IV-29.

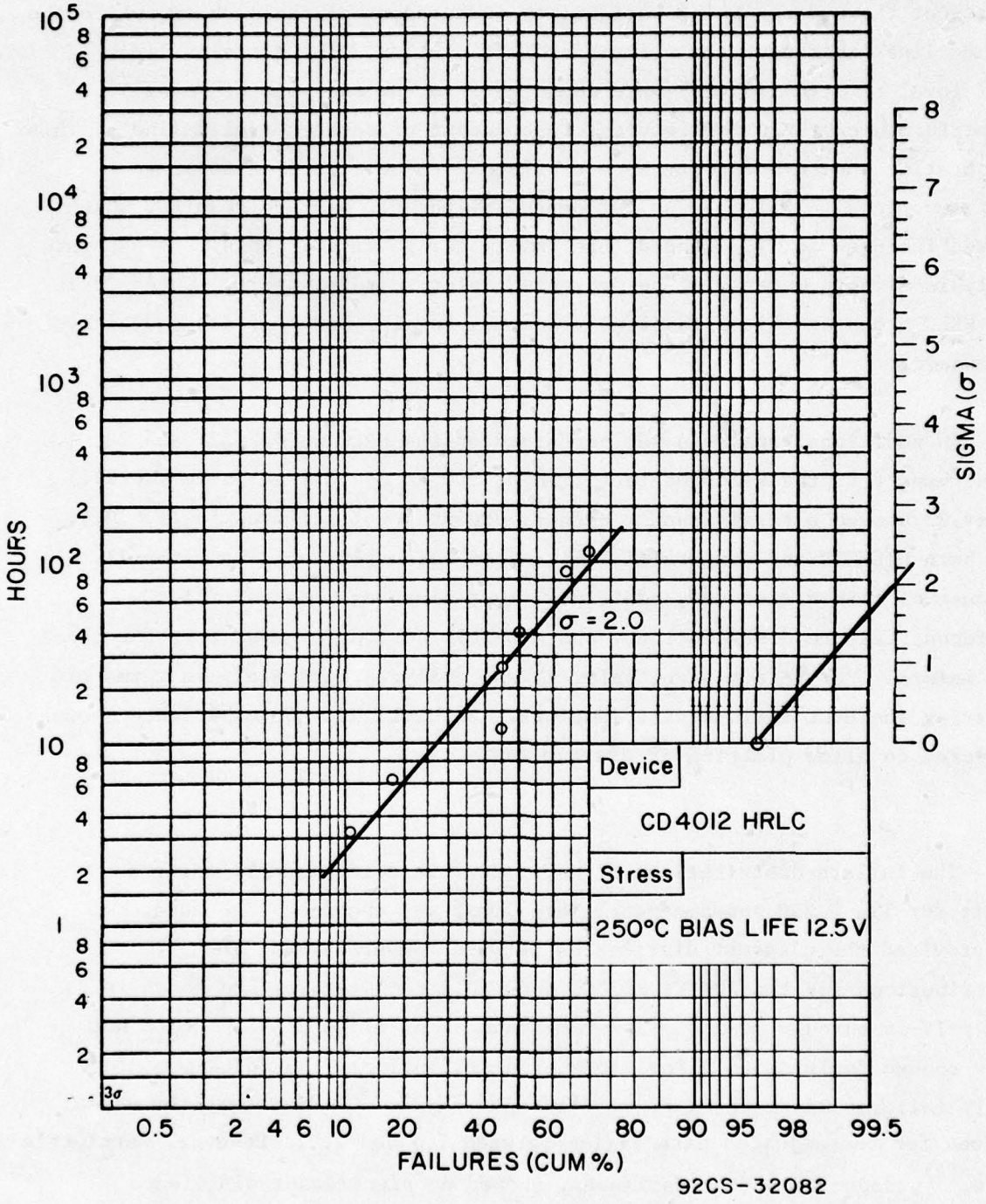

Fig. IV-26 - CD4012 HRLC, 250°C bias life, 12.5V ($I_{SS} \geq 250$ nA).

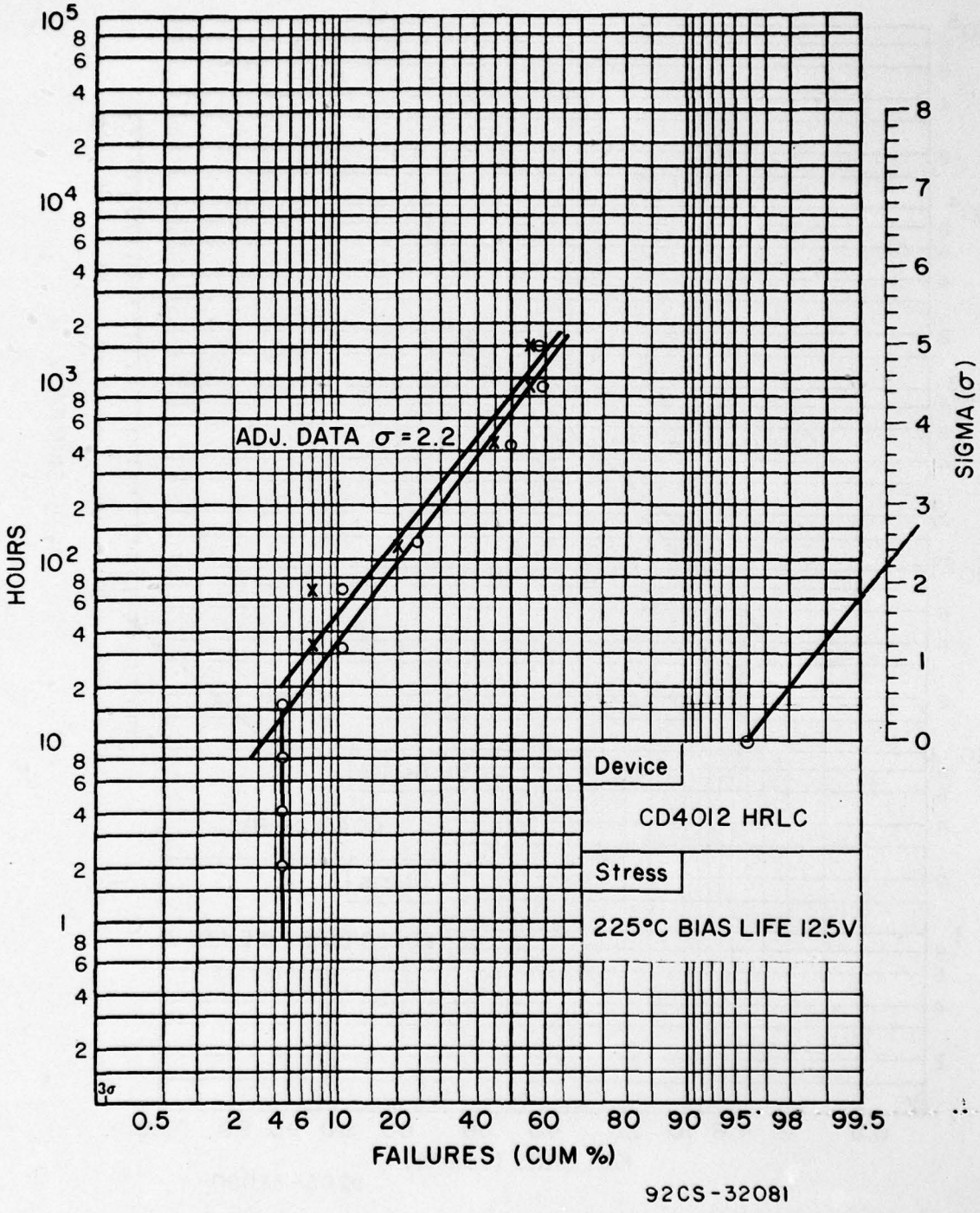

Fig. IV-27 - CD4012 HRLC, 225°C bias life, 12.5V ($I_{SS} \geq 250$ nA).

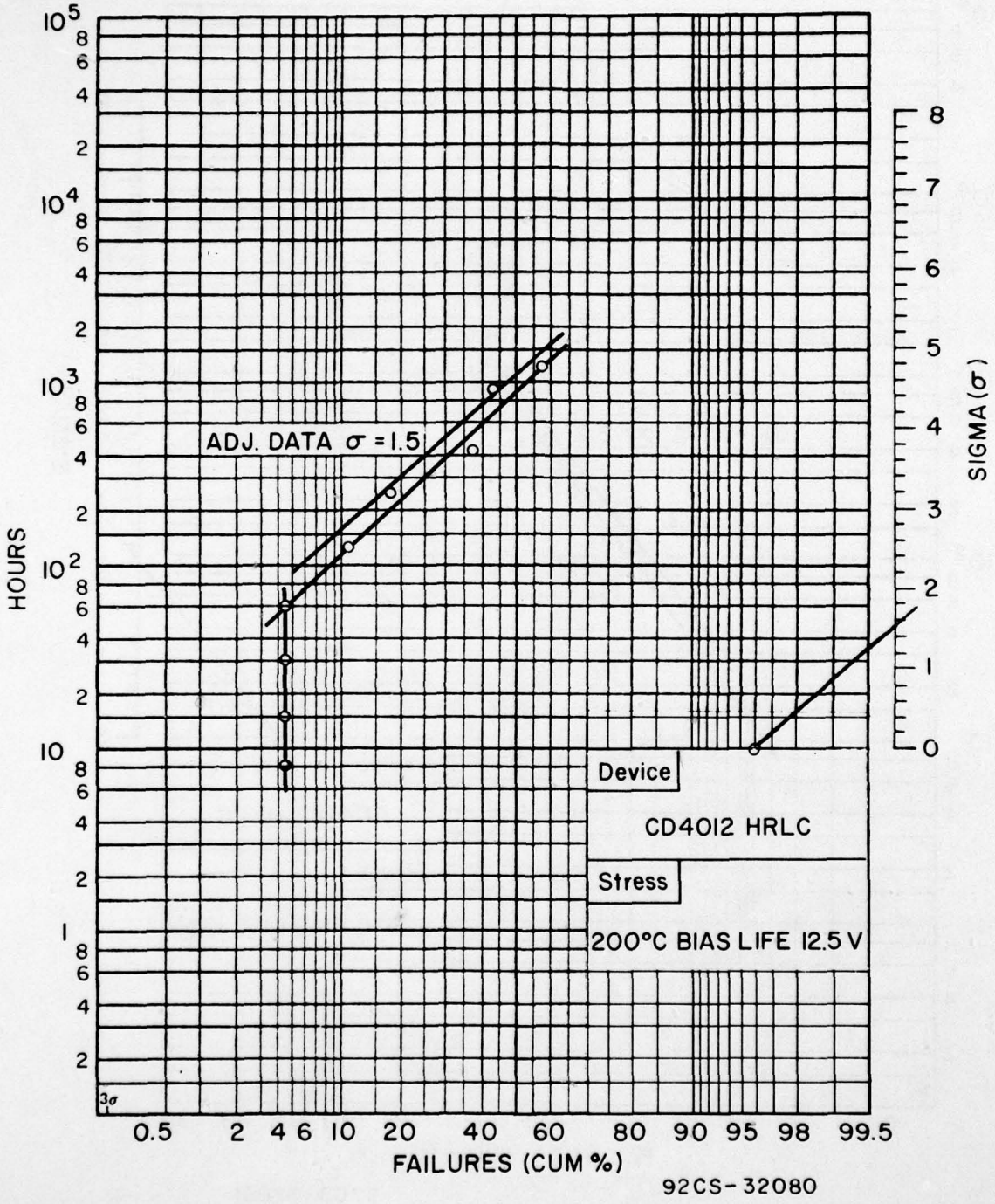

Fig. IV-28 - CD4012 HRLC, 200°C bias life, 12.5V ($I_{SS} \geq$ 250 nA).

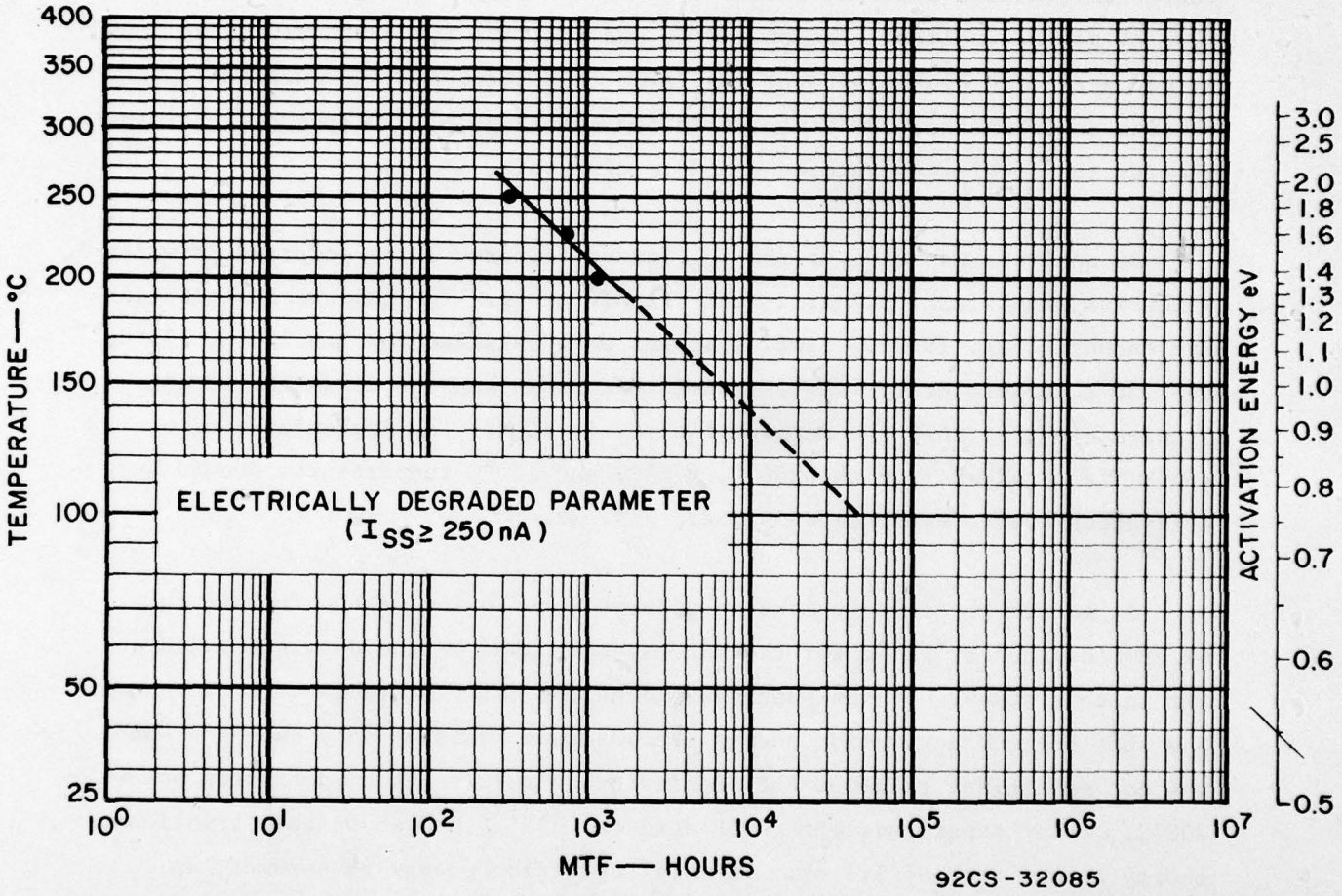

Fig. IV-29 - CD4012 auto dip (HRLC) bias life
12.5V (MTF on wafer No. 22).

Failure distributions were predicted for the 175°C and 150°C cases based on extrapolated MTF's using 0.55 eV and an average of the sigmas obtained at the higher temperatures. These predicted distributions are shown along with the higher temperature data in Fig. IV-30. At 175°C approximately 45% failures are predicted by 2000 hours; at 150°C approximately 25% failures are predicted by 1836 hours. However, the actual data at these temperatures shows no failures at these times. Thus, it appears that 0.55 eV is not applicable below 200°C, and that the data obtained above 200°C is not a true acceleration over the lower temperatures. The question remains as to whether 200°C itself is the cutoff point. Only additional test time at the lower temperatures can determine this.

An analysis was made of the V_{OH} loaded failures which occurred in wafer 5, which was significant primarily for the DIP group. The failure distributions are shown in Fig. IV-31. Similar slopes were obtained for the 250°C, 175°C, and 150°C temperatures. (It is noted that these samples consisted of only 5 units each, so that the margin of error is high.) An Arrhenius plot of the MTF's obtained from the 250°C, 175°C, and 150°C temperatures showed an activation energy estimate of 0.7 eV, Fig. 32.

It is not possible to make an accurate prediction of the failure rate of CMOS devices at 125°C for the HRLC system based on the data generated so far in this study. It has been shown that the data is highly wafer dependent and that the one activation energy obtained was based on only one wafer and was not sufficient to allow the prediction of results at temperatures below 200°C. Prior experience with CMOS devices [5,6,7] has shown an activation energy in the area of 1.2 eV. If this activation energy is assumed, an estimate of failure rate can be given using the 200°C data to extrapolate to 125°C. For a sigma value of 1.5 and an extrapolated MTF value of 4.5×10^5 hours, the failure rate is estimated to be about 0.005%/1000 hours using the $I_{SS} \geq 250$ μA criteria.

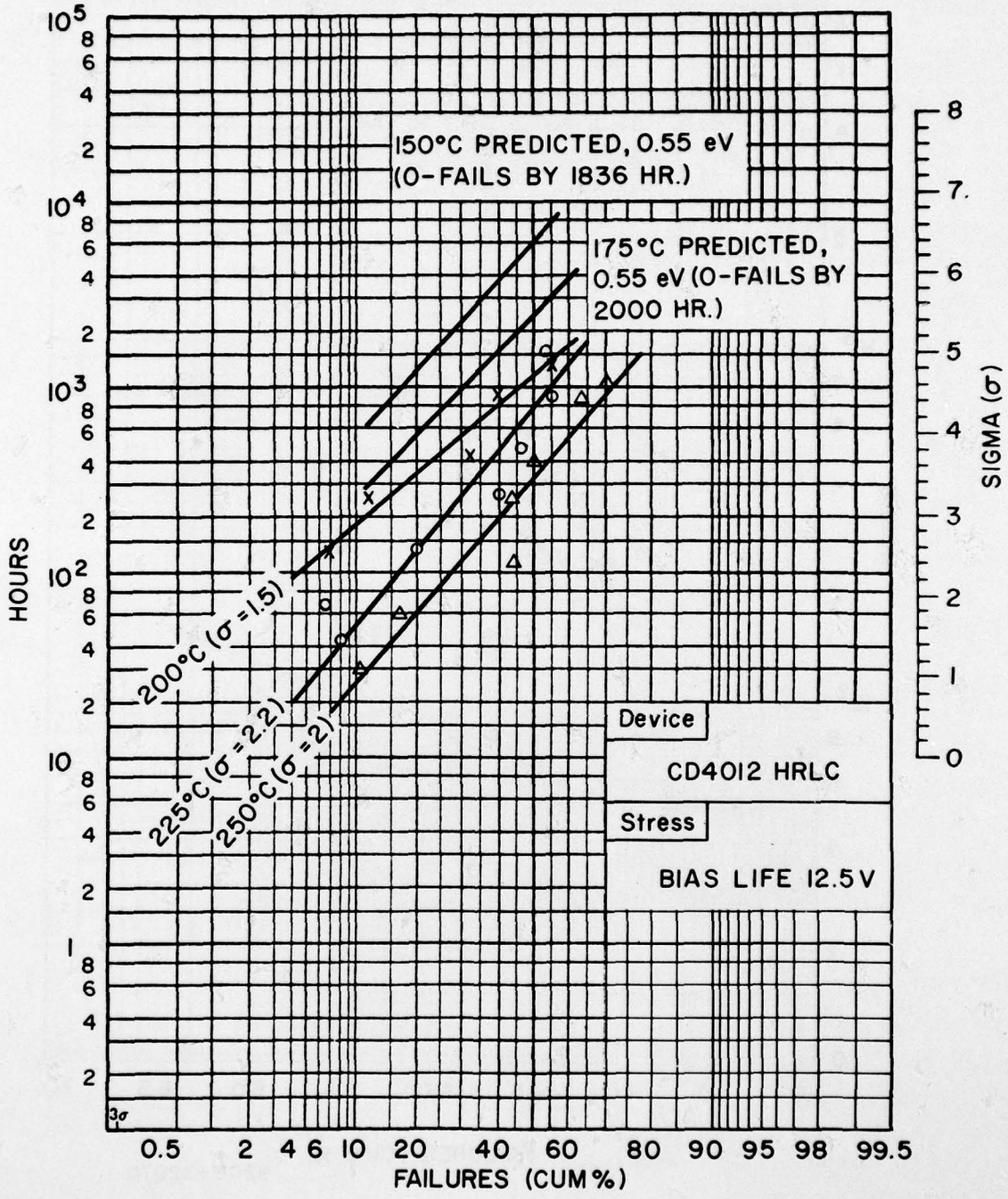

Fig. IV-30 - CD4012 HRLC, bias life, 12.5V ($I_{SS} \geq 250$ nA).

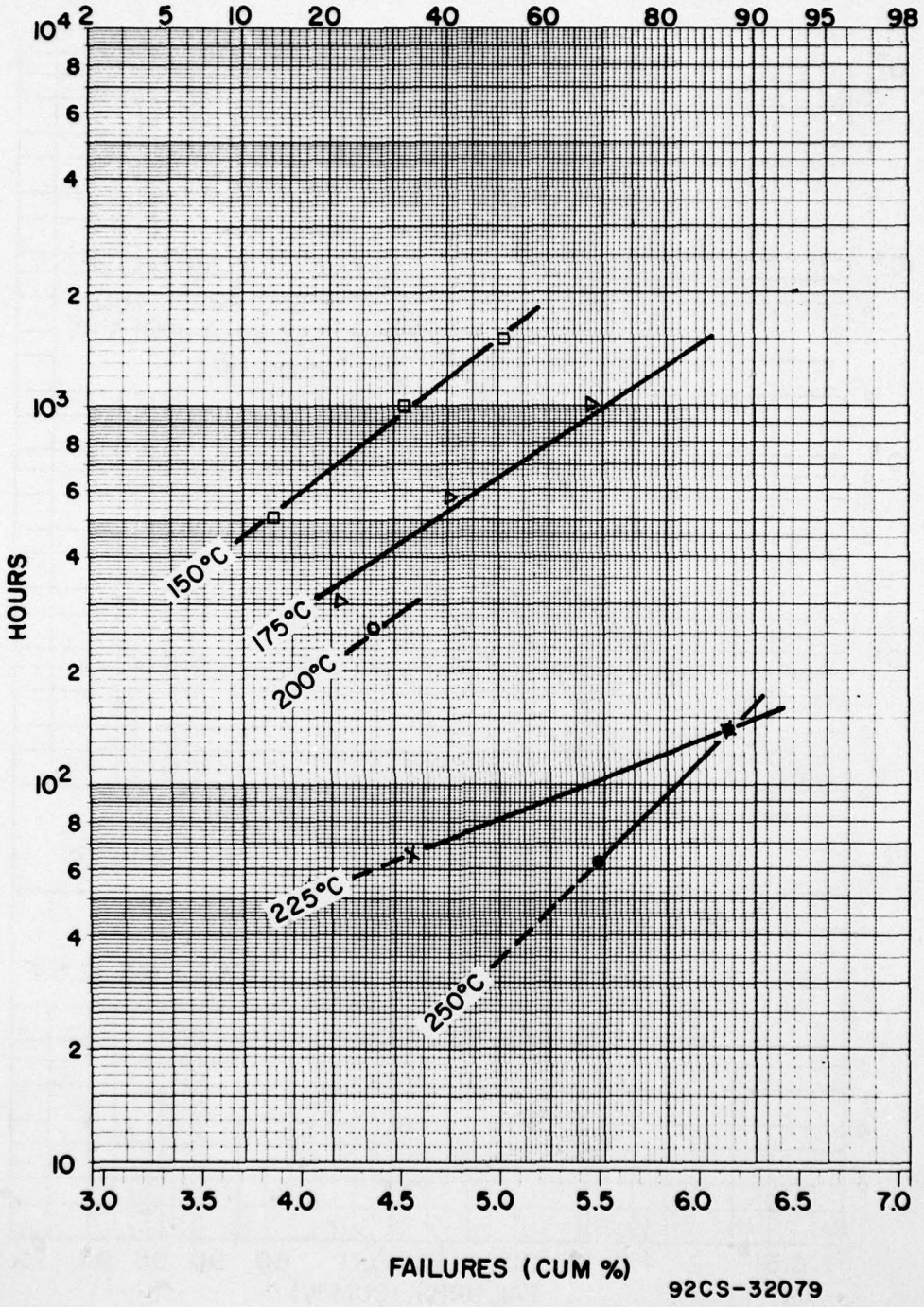

Fig. IV-31 - CD4012 wire bonded, bias life, 12.5V, inputs low, wafer No. 5, N=5 each temperature (V_{OH} loaded).

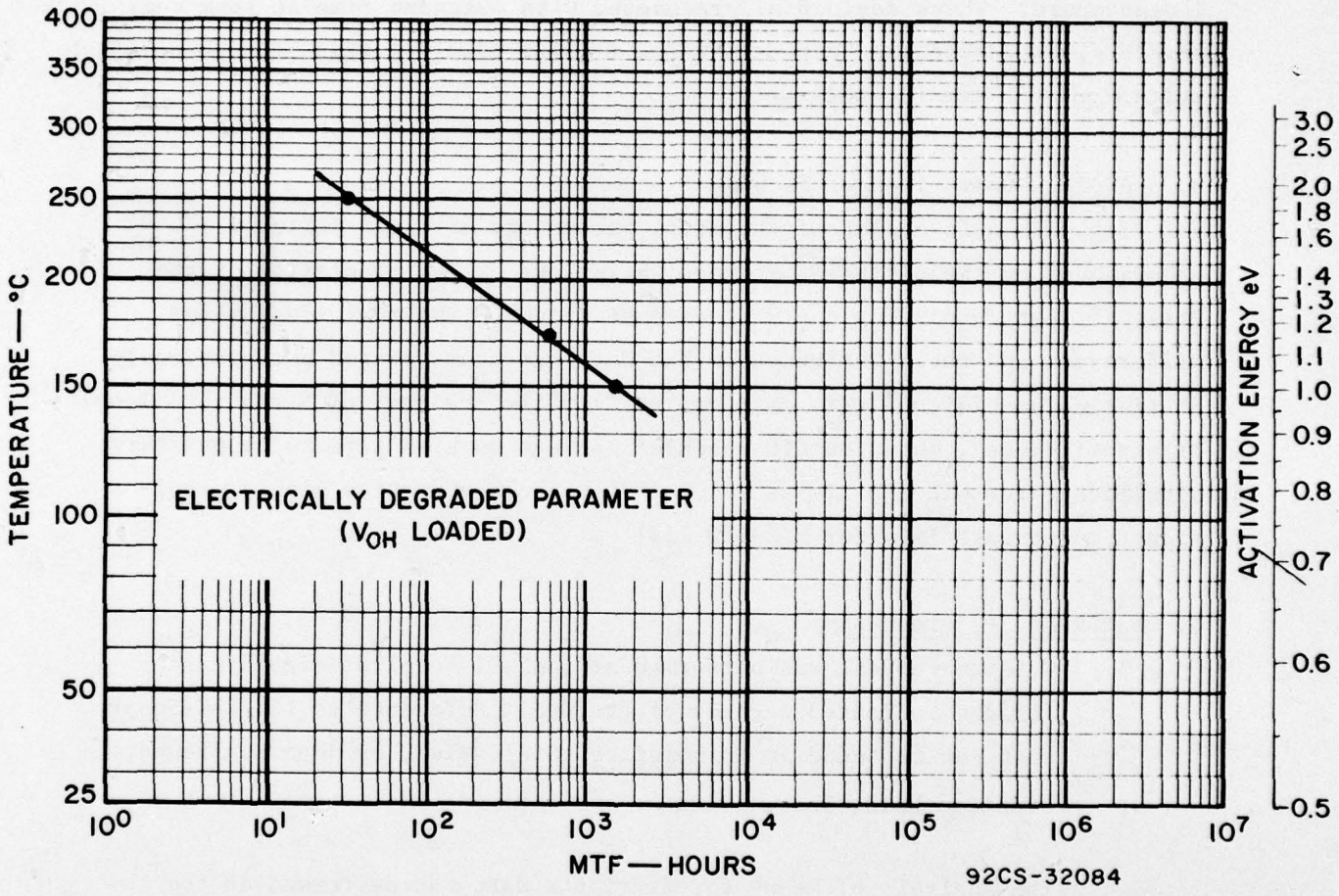

Fig. IV-32 - CD4012 wire bonded, bias life, 12.5V, inputs low, wafer No. 5, N=5 each temperature.

7. CD4012 - Storage-Life Results

A summary of the data is shown in Tables IV-23, IV-24, IV-25, and IV-26. This data shows a significantly high percentage of MIL-STD limit failures occurring in the DIC package at 157°C and 150°C and in the DIC unsealed package at all temperatures. A plot of this data is shown in Fig. IV-33. These failures were marginally over the MIL-STD limit, primarily in I_{IL} at 1 nanoampere. These devices all recovered with extended time at room temperature. No cause has been determined at this time for this phenomenon which occurs only in the DIC packages.

8. CA4012 - Comparison of Package Systems

Fig. IV-34 is a plot of the total percentage of limit failures experienced by the different package variations at the completion of the Phase II test (excluding the HRLC extended time). The individual wafer differences and their influence on the data has been pointed out previously. Statistical decision lines, as computed from the Analysis of Means (.01 level of significance), show the DIC unsealed package on bias life to be possibly significant for MIL-STD limits and both DIC package systems highly significant on storage life for MIL-STD limits.

9. Notes And References

1. Chi-Square Test was performed at the .01 level of significance for the indicated degrees of freedom. Reference to the Chi-Square test can be found in Mathematical Statistics, by John E. Freund, Prentice-Hall, Inc., 1962.

2. The Analysis of Means for attribute data was performed at the 0.1 level of significant. A discussion of the Analysis of Means is found in Process Quality Control, by E. Ott, McGraw-Hill, Inc., 1975.

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Table IV-23

NAVELEX DATA SUMMARY - PHASE II

Type and Description CD4012 Auto Dip (HRLC) Test Storage Life

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=29)			225°C (N=30)			200°C (N= 30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	0	0	2	0	0	2	0	0	8	0	0	8	0	0
4	0	0	4	0	0	4	0	0	24	0	0	24	0	0
8	1	0	8	0	0	8	0	0	168	0	0	168	0	0
16	0	0	16	0	0	16	1	0	336	0	0	500	0	0
32	0	0	32	0	0	32	0	0	672	0	0	1000	0	0
64	0	0	64	0	0	64	0	0	1000	3	0	1500	0	0
128	0	0	128	0	0	128	0	0	1344	0	0	2000	0	0
256	0	0	256	0	0	256	0	0						
Total	1	0		0	0		1	0		3	0		0	0

RCA

Table IV-24

NAVELEX DATA SUMMARY - PHASE II

Type and Description CD4012 DIP Wire Bonded Test Storage Life

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=30)			225°C (N=30)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	-	-	2	-	-	2	-	-	8	-	-	8	-	-
4	-	-	4	-	-	4	-	-	24	-	-	24	-	-
8	-	-	8	-	-	8	-	-	168	-	-	168	-	-
16	-	-	16	-	-	16	-	-	336	1	0	500	2	2
32	0	0	32	3	0	32	5	0	672	0	0	1000	0	0
64	1	0	64	1	1	64	0	0	1000	1	0	1500	0	0
128	0	0	128	0	0	128	0	0	1344	0	0	2000	0	0
256	0	0	256	0	0	256	0	0						
Total	1	0	/	4	1	/	5	0		2	0	/	2	2

RCA

Table IV-25

NAVELEX DATA SUMMARY - PHASE II

Type and Description CD4012 DIC Wire Bonded **Test** Storage Life

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N=30)			225°C (N=28)			200°C (N=30)			175°C (N=30)			150°C (N=30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	-	-	2	-	-	2	-	-	8	-	-	8	-	-
4	-	-	4	-	-	4	-	-	24	-	-	24	-	-
8	-	-	8	-	-	8	-	-	168	-	-	168	-	-
16	-	-	16	-	-	16	-	-	336	3	0	500	2	0
32	2	0	32	4	0	32	1	0	672	0	0	1000	2	0
64	1	0	64	0	1	64	0	0	1000	0	0	1500	15	0
128	2	1	128	0	0	128	0	0	1344	27	0	2000	11	0
256	3	0	256	0	0	256	4	0						
Total	8	1		4	1		5	0		30	0		30	0

RCA

Table IV-26

NAVELEX DATA SUMMARY - PHASE II

Type and Description CD4012 DIC (Unsealed) Wire Bonded Test Storage Life

Number of Devices Exceeding Mil-Std and Commercial Limits at Each Down Time														
250°C (N= 30)			225°C (N= 30)			200°C (N=30)			175°C (N=30)			150°C (N= 30)		
Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com	Hrs.	Mil	Com
2	-	-	2	-	-	2	-	-	8	-	-	8	-	-
4	-	-	4	-	-	4	-	-	24	-	-	24	1	1
78	-	-	78	-	-	8	-	-	168	-	-	168	0	0
94	1	0	94	0	0	16	-	-	336	1	0	500	0	0
128	6	0	128	1	0	32	0	0	672	1	0	1000	2	0
256	14	1	256	18	0	64	2	1	1000	22	0	1500	13	0
						128	2	0	1344	0	1	2000	10	0
						256	10	0						
Total	21	1		19	0		14	1		24	1		26	1

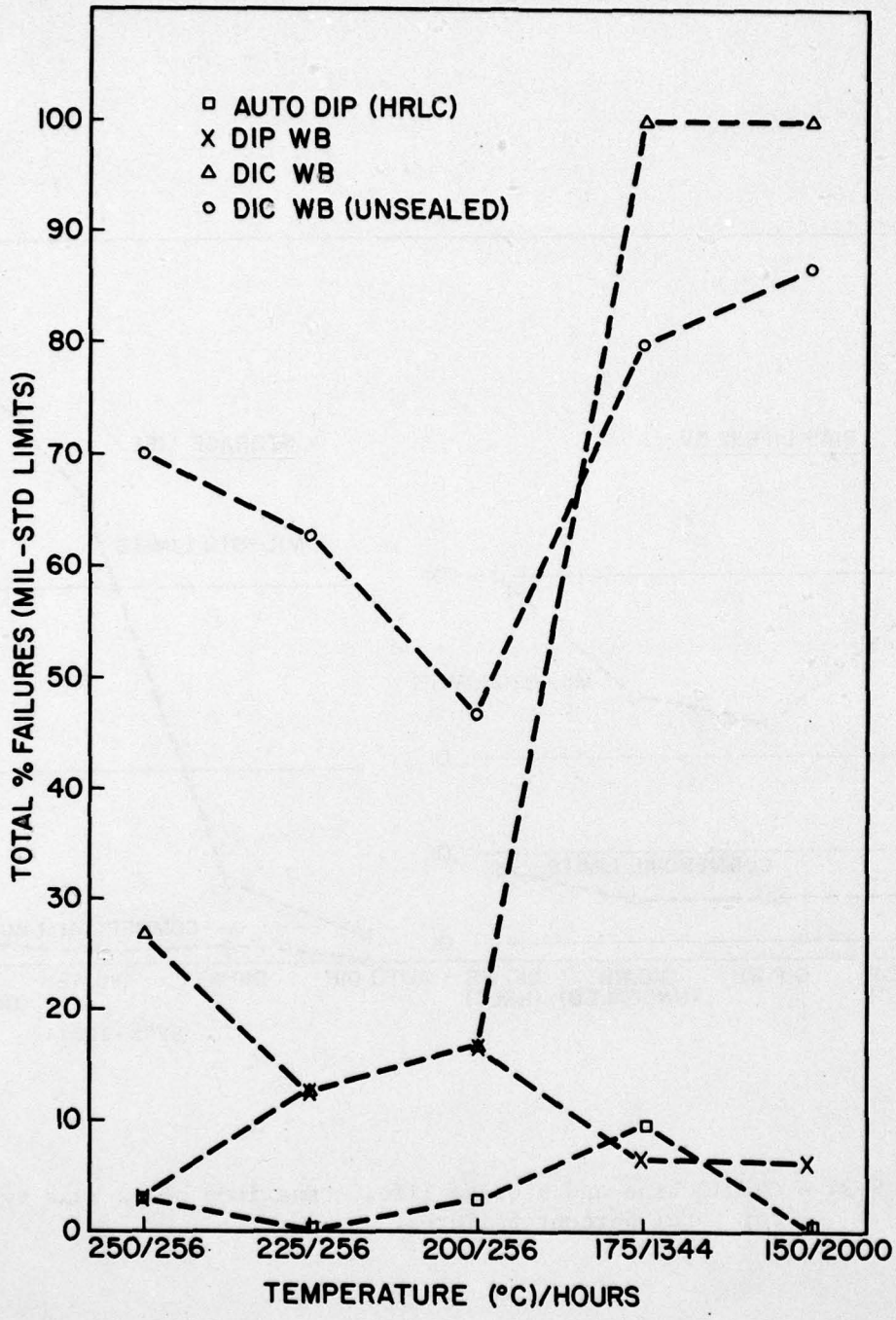

Fig. IV-33 - CD4012 storage life, comparison of package systems for total percent failures with temperature (MIL-STD limits).

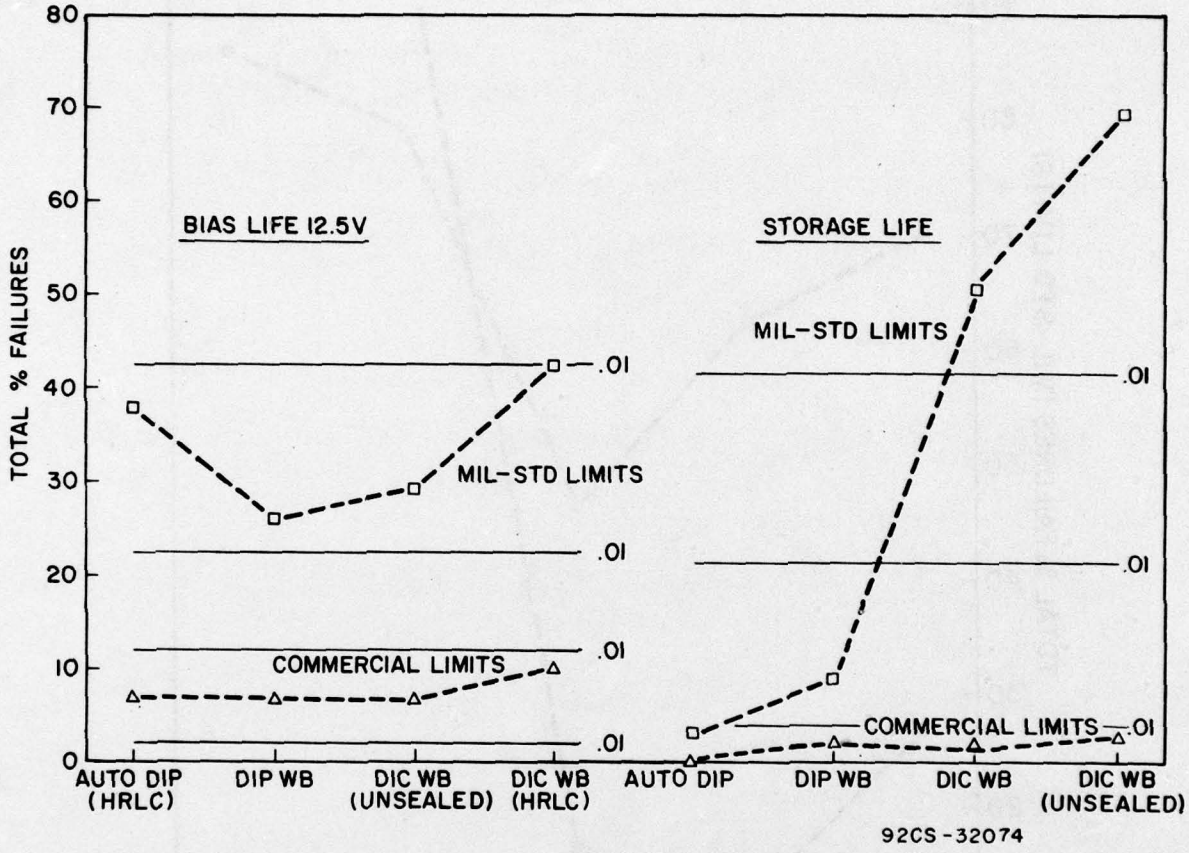

Fig. IV-34 - CD4012 bias and storage life, comparison of package systems for total percent failures.

3. The data was adjusted from the following formula:

$$M_P = \frac{T_P - F_P}{1 - F_{P/100}}$$

where, M_P = Percentage in the main distribution

T_P = Percentage in the total distribution (raw data)

F_P = Percentage in the freak population (early failures).

4. Bartlett's Test on the Homogeneity of Variances was performed at the .01 level of significance. A discussion of the test can be found in Quality Control and Industrial Statistics, by A. J. Duncan, Richard D. Irwin, Inc., 1965.

5. "Predicting the Reliability of Integrated Circuits and Discrete Power Devices," by L.J. Gallace, RCA Technical Reprint ST-6477.

6. "Reliability Considerations for COS/MOS Devices," by L.J. Gallace and H.L. Pujol, RCA Technical Reprint ST-6418.

7. "Accelerated Testing of COS/MOS Integrated Circuits," by L.J. Gallace and C.D. Whelan, RCA Technical Reprint ST-6379.

AD-A081 666 RCA SOLID STATE DIV S. MERVILLE NJ F/G 9/5
PHASE II FINAL DEVELOPMENT REPORT FOR HIGH-RELIABILITY, LOW-COS--ETC(U)
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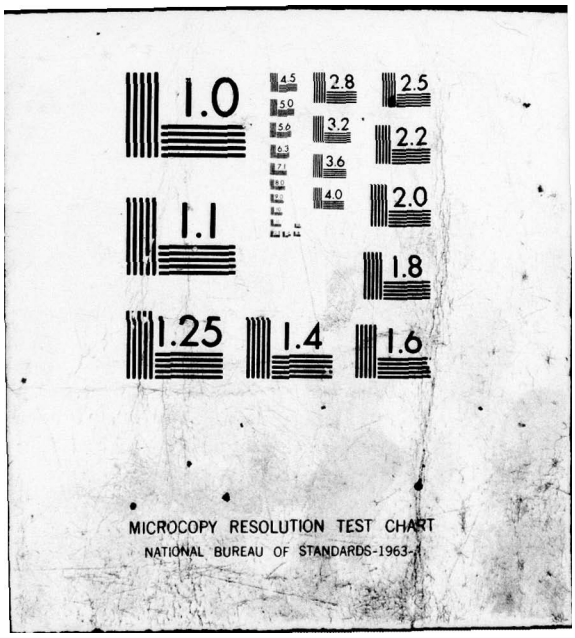

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
7.1
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

F. Analysis of Units Out of Specification From Phase II Life Tests

1. Introduction to Phase II Analysis Philosophy

Units out of specification at down period computer testing were retested after several weeks of storage at room temperature. Units with parameters outside commercial product test limits were chosen for detailed device analysis. Units beyond commercial limits have more distinct anomalies enabling more definite conclusions. Units with parameters borderline to the MIL specs probably have the same mechanisms to a lesser degree.

Since the main concern of this contract is the beam-tape plastic-molded (HRLC) units, all of these HRLC units outside commercial limits were analyzed in depth while representative samples were analyzed from units on the other package test cells. A tabular summary of devices analyzed will be found below.

2. Highlights of Analysis Procedure

a. Pin Checking - Before decapsulation (decap) of the silicone molded (DIP) units or the delidding of the ceramic (DIC) units, all units were given a pin-by-pin check using a Tektronix Model 576 curve tracer. These pin checks, generally regarded as good practice, detected approximately 20 units with broken or folded-under package leads. After repair, most of these units were in specification. The CD4012B units were pin checked with each pin, in turn, biased negatively and positively against all the other pins. The pin check serves as an adjunct to the computer tester. For example, the CD4012 unit No. 10 from cell 3 of the computer printout showed I_{IH} on pin 7 out of spec. The pin test showed pin 7 to be intermittent. Inspection of the unit revealed that the open pin 7 conductor path was the result of a cracked ceramic.

The CA741G units are pin checked with each pin biased negatively and positively with respect to pin 6 (V-) alone; then with each pin biased with respect to pin 11 (V+) alone. After several decapped HRLC 741's were observed to have beams lifted from the chip contact pads, a heating and cooling step was introduced while each pin was under curve tracer bias.

An intermittent pin-10 beam on unit No. 5 of cell 1A (HRLC on 250°C BL) was detected by this short thermal stress.

b. Decapping/Delidding - The silicone molded units, both HRLC and wire-bonded construction, were decapped for analysis by grinding a cavity part way to the chip, then dissolving the plastic remaining over the chip in hot tetramethylguanidine for about 30 minutes. It was observed on the HRLC units that the CD4012 CMOS units had virtually no lifted beams after decap while the HRLC CA741 units had no unit with all the beams in contact after decap. Two of the reasons for this occurrence are: (1) the CD4012 has 3 beams per side or 12 beams total while the CA741 has 3 sides with only 2 beams each with a total of 9 beams/chip; (2) since the CA741 electrical tests are considerably more sensitive to contact resistance than the CD4012's, more 741's with marginal beam contacts would be called out for analysis. However, probably of greater significance are the SEM views of metal surfaces where the beam and chip were originally in contact, views which indicate that the bonding on the lifted beam was metallurgically superficial. These photos are included in a section, below, on failure mechanisms.

Delidding of ceramic DIC packages is quickly accomplished by using a razor blade to shear the cap weld ring off the ceramic at the metallizing joint. The blade is driven parallel to the top surface of the package.

c. Fault Location and Isolation - An experienced analyst can usually narrow down the possible anomalous sites on the COS/MOS CD4012's to a diode network and a small number of MOS transistors based on computer or bench electrical test data. To further pinpoint the exact anomalous device on standard aluminum metallization units, micromanipulation probes are used to scribe-isolate suspect devices and probe test these devices. The contract units all have titanium-plantinum-gold (trimetal) metallization, which is considerably more difficult to isolate by scribing than aluminum metallization. The isolation method used on these Phase II units was as follows:

1. At the site in the metal run where a "cut" was needed, the silicon nitride over the run was punctured by a probe. Etching will take place at these puncture sites while the rest of the chip is masked by the nitride layer.
2. The top gold layer at the puncture site is removed in Halma etch (commercial iodide gold etch) in about 2 minutes.
3. The platinum layer was mostly etched off in warm aqua regia - time, approximately 2-4 minutes.
4. The titanium layer was removed in 90 seconds of buffered-oxide etch.
5. Any metal residues in the "cut" were scribed away by the micro-probe.

Once the suspect devices, diodes or MOS transistors are isolated, they are probe tested using a Tektronix Model 576 curve tracer. Depending on the leakage, breakdown voltage V_T, etc. of the device, compared to normal devices and compared to the test circuit requirements, a judgement is made as to whether that anomalous device is the key fault location. The electrical behavior of this device is then monitored during metal etches, oxide etches, rinses, and/or bakes as a basis for conclusions as to the cause of the anomaly. In the case of pinpoint oxide shorts, high-power visual inspection as the device is "delayered" will help in an understanding of the exact location and the amount of energy involved.

Fault-site location on the CA741, other than obvious visible anomalies, required operation of the open IC as an amplifier and active probing for voltage at key circuit nodes. These node voltages are compared to readings on reference units which are in specification. The voltage node data will usually indicate which subsection of the IC should be investigated more thoroughly. The suspect section of the unit will then be 2-point probed (unit not under operating bias) and the curve tracer characteristics compared with those of a reference unit.

The individual diodes, transistors, etc. in any part of the circuit showing an anomalous trace will be isolated by the trimetal puncture and etch method previously described in this section and probe tested. Here again, the search will be for a device with parameters below normal capabilities and below test-circuit requirements. Depending on the electrical characteristics of the individual device after etching, rinsing, and for baking, a conclusion will be drawn as to the root cause of the anomaly.

3. Significant Failure Modes and Mechanisms

a. CD4012 - The largest single failure mechanism in units analyzed was the V_{DD}-V_{SS} metallization burns; all from cell 1D (HRLC-175°C BL) at the 168-hour down-period test. Based on previous experience these burns are the result of reversed socketing at testing, an operator error.

While only two V_{OHL} (output high voltage, loaded) failures were analyzed in depth, their results were clearcut and representative of several other low V_{OHL} units, these other low V_{OHL} units come from various bias-life test cells, and both plastic and ceramic packages. In verifying V_{OHL} with a bench test, it was noted that with certain inputs set low, the V_{OHL} was lowest (typically 2 to 3 volts instead of 4.2 volts). As a result of isolating and probing the PMOS devices connected to these inputs, the threshold voltages (V_T) were found to be 3.1 volts and 3.5 volts (a typical V_T is 1.4 volts), and the source-drain breakdown voltage showed a rapid increase with applied voltage. A 2-hour 150°C bake of one unit reduced V_T from 3.1 to 2.8 volts and increased breakdown from 5 to 25 volts. These data indicate an excessive number of mobile positive charges in the PMOS gate oxide. This result could also possibly explain some of the borderline failures of I_{SS} and I_{IL}.

b. CA741 - The largest 741 failure mode is out-of-specification V_{IO}, input offset voltage. V_{IO} is an indication of overall amplifier circuit performance. It was noted that cell 1A, the HRLC 250°C BL group, had the heaviest concentration of out-of-specification V_{IO} compared with only a few units in the wire-bonded plastic cells.

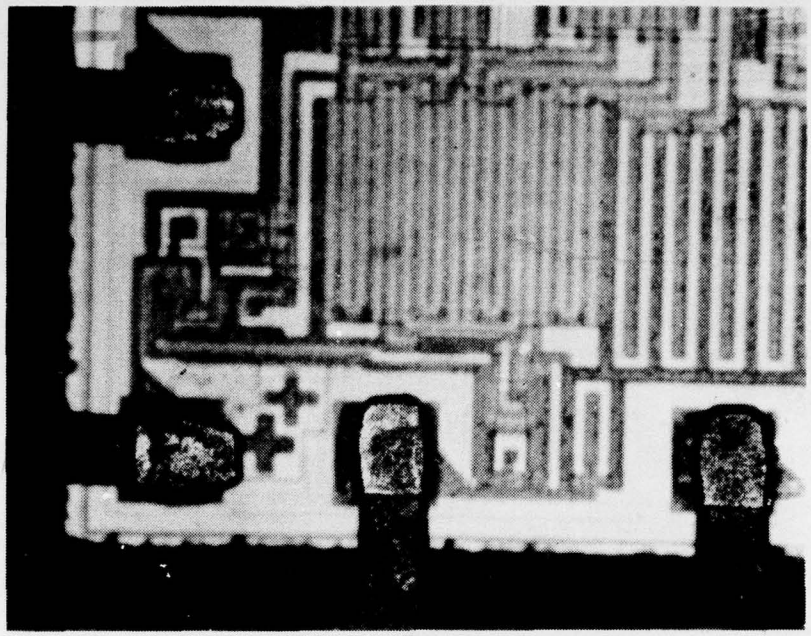
After the HRLC CA741's had been decapped in hot guanidine, it was noted that every unit had at least one open beam-to-chip bond, and usually more than one. By mechanically holding the loose beam in contact, by silver epoxying the loose beam contact, or by remounting and wire bonding these 1A units, all were retested in specification for V_{IO}. To further show the difference between the failure mechanisms for the HRLC and wire-bonded plastic construction, one of the wire-bond units, out of specification for V_{IO}, was found to have a shorted C-1 capacitor.

Based on the high incidence of devices out of specification for V_{IO} for the HRLC compared to the wire-bond DIP's, and the recovery for HRLC with the re-establishment of good beam contact, the conclusion is that the major cause of failure was marginal beam-to-chip bond contact.

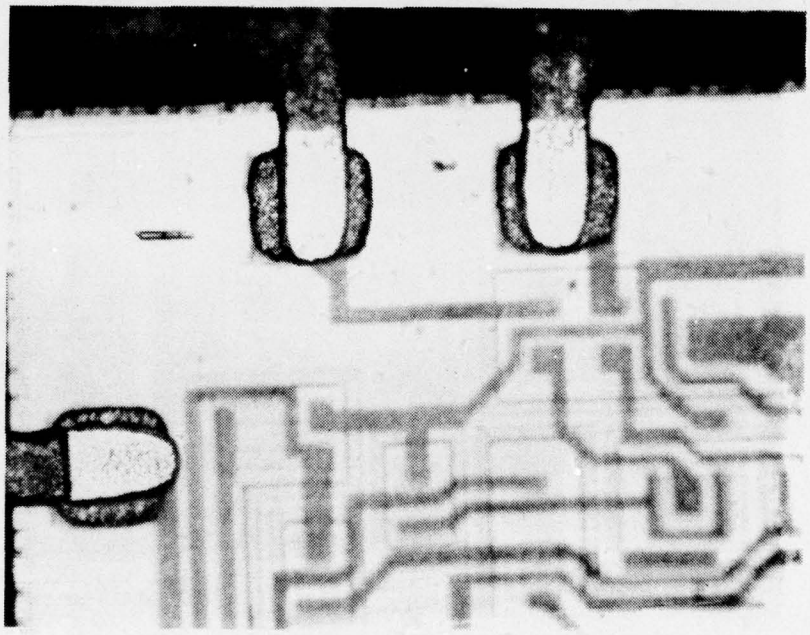
Further investigation into the beam-to-chip bonding led to comparison of the CD4012 and CA741 beam deformations. Figs. IV-35(a) and IV-35(b), microphotographed at the same magnification, show typical configurations for beams, at the chip bond. Judging from the lateral deformation (width) of the beams the CD4012's had slightly more effective pressure than the CA741's.

Figs. IV-36(a) and IV-36(b) show 100X and 150X SEM views of the CA741 chip pads which had lifted beams after decap. The degree of metal-to-metal bonding appears to be metallurgically superficial. Fig. IV-36(b) shows where the beam was aligned with only half of pad 10. While Fig. IV-36(b) is the worst case in this group of units, Fig. IV-36(a) is typical of the CA741 pads with beam lifts in Phase II.

Table IV-27 describes analysis results of all failed devices tested under the Navelex program.

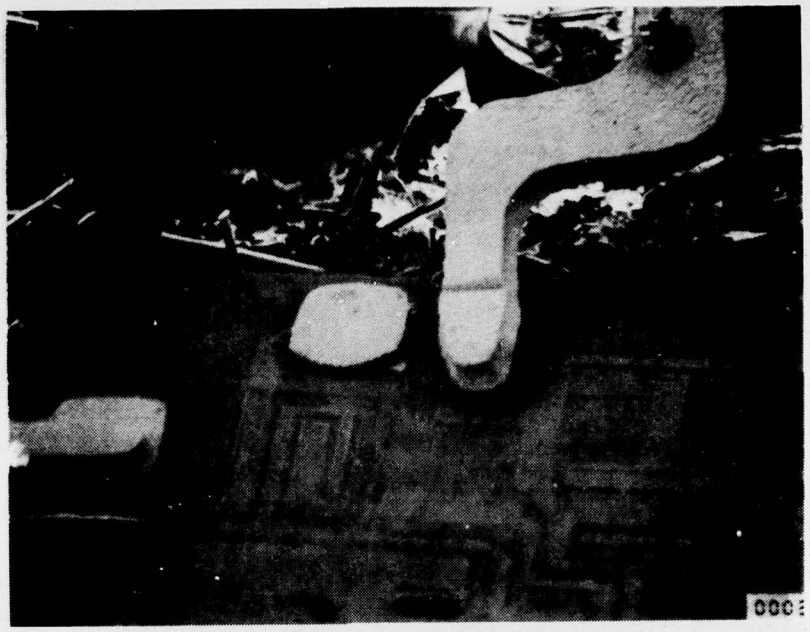


(a) Typical CD4012 beam deformation (cell 1D, unit No. 27).

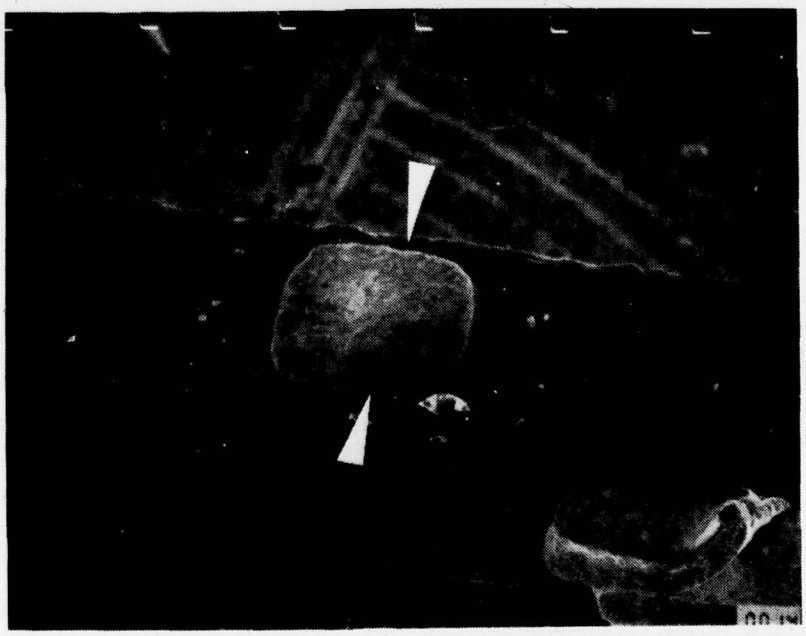


(b) Typical CA741 beam deformation (cell 1A, unit No. 4).

Fig. IV-35



(a) CA741, cell 1A, unit No. 5, 100X SEM Post Decap, pad 11, showing superficial metal bonding at interface.



(b) CA741, cell 1A, unit No. 6, 150X SEM, pad 10, showing superficial bonding to the left of arrows and no deformation to the right of the arrows.

Fig. IV-36

Table IV-27

NAVELEX DEVICE ANALYSIS RESULTS

CD4012

CELL	UNIT NO.	OUT OF SPEC PARAMETER	TEST HOURS	SUMMARY OF ANALYSIS
1B HRLC 225°C BL	30	IIL(pin 12)=26.7nA ISS=0.6μA	16	Pin 12 protect diodes and pin 12 NMOS tested normal. The pin 12 PMOS was damaged during isolation cuts. Location and cause of leakage not determined.
1C HRLC 200°C BL	20	IIH(all)=21.5nA IIL(pin 10)=188nA	4	Leakage decreased to within spec during room temperature storage after the computer verification test.
1D HRLC 175°C BL	10	ISS=200μA	8	VDD metal shorted through an oxide pinhole to a VSS region.
	25	VSS, high resistance	168	Burn on VSS metal run, current overstress.
	26	Shorted inputs	168	High current overstress between VDD and VSS.
	27	VSS, high resistance	168	Burn on VSS metal run, current overstress.
	28	VSS, open	168	VSS metal run burned open, current overstress.
	30	VSS, high resistance	168	Burn on VSS metal run, current overstress.
				Units 26, 27, 28, 30 were similarly exposed to current overstress at the 168 hour down period. A probable cause is reversed socketing during testing.
2A DIP Wire bond 250°C BL	12	VOHL=2.2V	128	Damaged during decap; cause not determined.
	13	VOHL=2.0V	128	Pin 5 PMOS had a threshold leakage of 3.5V and a breakdown voltage "walkout" indicating excessive positive charge in the gate oxide.
	27	IIH=1.2μA		Leakage of 2μA at 15V located at pin 4 input resistor to VDD; 2 hour 150°C bake no change. Degraded breakdown caused by electrical overstress.

Table IV-27

NAVELEX DEVICES ANALYSIS RESULTS (cont'd)

CD4012 (Cont'd)

CELL	UNIT NO.	OUT OF SPEC PARAMETER	TEST HOURS	SUMMARY OF ANALYSIS
2B DIP Wire Bond 225°C BL	13	VOHL=2.17V	256	Pin 12 PMOS had a threshold voltage of 3.1V & a 5V breakdown voltage. A 2 hr. 150°C bake lowered the threshold voltage to 2.8V and increased breakdown to 25V. This indicates excessive mobile positive charge in the gate oxide.
2C DIP Wire Bond 200°C BL	5	ISS=0.8mA IIL multiple	2	VDD, VSS, and pin 9 metal runs were fused together at the input diode network. Cause of shorts: electrical overstress on pin 9.
2D DIP Wire Bond 175°C BL	2	IIL=1.8μA (pin 4)	7	Leakage of 1μA at 15V located at pin 4 NMOS gate tunnel. Leakage cleared during isolation metal etches. Cause: unknown surface contaminant.
	6	VDD shorted to VSS	7	Burn on VSS metal run, current overstress. Probable cause: reversed socketing at test.
3B DIC 225°C BL	10	Pin 7, intermittent open	8	Pin 7 package conductor run was open due to crack in ceramic body.
3D DIC 175°C BL	27	ISS=65μA	168	Gate to source short on pin 9 NMOS. Short cleared with metal etches. Cause of short: voltage overstress on pin 9.
3E	3	ISS=2mA VOL=1.4V	1000	Pins 5 and 10 package conductor runs were open due to cracks in the ceramic package body.
3F DIC 250°C SL	30	ISS=2mA	128	Pin 5 was open due to bond lift at the package.
4A DIC (Unsealed) 250°C BL	19	ISS=4.4μA	64	Pin 11 PMOS had 4.4μA of inversion leakage at 8V. No shift with 16 hour 150°C bake. Cause of leakage: localized oxide contamination.
	21	ISS=20μA	64	Leakage cleared with removal of oxidation on the external lead causing a near open on the pin 11 input.
4B DIC (Unsealed) 225°C BL	12	IIL=14μA	256	Bond wires were physically deformed and touching the edge of the chip. Leakage cleared by reshaping the bond wires.

Table IV-27

NAVELEX DEVICES ANALYSIS RESULTS (cont'd)

CD4012 (Cont'd)

CELL	UNIT NO.	OUT OF SPEC PARAMETER	TEST HOURS	SUMMARY OF ANALYSIS
4E DIC (Unsealed) 225°C BL	1	ISS=2mA IIH=83μA	1500	Most of the leakage cleared with the repair of a missing external lead. Minor leakage in the pin 4 diode network cleared with metal and oxide etches. Cause: unknown contaminant.
	17	IIL=20μA	500	Pin 9 package conductor run was open due to a crack in the ceramic package body.
	24	ISS=2mA	1580	Bond wires were physically deformed and touching the edge of the chip. Leakage cleared by reshaping the bond wires.
4J DIC (Unsealed) 150°C SL	11	IIL=0.8μA (pin 9)	1000	Gate oxide short, pin 9 PMOS gate to source; cause VDD voltage overstress.
CA741				
1A HRLC 250°C BL	2	VIO=-17.8mV (clamp value)	1500	Beams lifted from chip during decap. Retest after epoxy remount and bake: VIO= 0.72mV. Cause of out of spec condition: marginal beam to chip contact.
	4	VIO=+12mV	32	After decap, pin 10 beam lifted from the chip. By holding the pin 10 beam down with a probe, the unit was VIO tested at 1.8mV. Cause of the out of spec VIO: marginal beam to chip contact.
	5	VG=14.08 (Limits -1.0 to +1.0)	512	Pin check during heating and cooling showed pin 10 (output) to have an intermittent contact. After decap it was observed that pin 10 beam was not attached to the chip. From the appearance of the interface the beam to chip bond was marginal.
	8	VIO=+16.6mV	1500	Decapping, 2 beams were lifted from the chip. Unit was remounted in a DIC package, baked at 200°C for 2 hours, and rebonded. Retest on VIO -0.07mV. Cause of out of spec VIO: marginal beam to chip contact.
	16	Open pin 12	128	Pin check showed open pin 10. Post decap visual showed a pin 10 beam lift at the chip. SEM analysis showed only half the chip pad was deformed. Cause of open: marginal beam bond to chip.

Table IV-27

NAVELEX DEVICES ANALYSIS RESULTS (cont'd)

CA741 (Cont'd)

CELL	UNIT NO.	OUT OF SPEC PARAMETER	TEST HOURS	SUMMARY OF ANALYSIS
	18	VIO=+16.6mV	1500	Pin check with heating and cooling was normal. Decapping showed pin 10 beam to be lifted from the chip. Retesting after repairing the bond with silver epoxy and baking for 2 hours at 150°C VIO=0.01mV. Cause of out of spec VIO: marginal beam to chip contact.
	21	VIO=+8mV	256	After decap, 3 beams had lifted from the chip; pins 3, 10 and 11. In order to operate the unit during active probing; silver epoxy was applied to the open bonds and baked at 150°C for 2 hours. Post bake pin check showed pin 3 had continuity; pins 10 and 11 were still opens. While socketed for VIO testing, 2 microprobes were used to hold the pin 10 and 11 beams in contact. VIO read -1.5mV. Cause of out of spec VIO: marginal beam to chip contact.
	24	VIO=+8.98mV	128	After decap, one of the beams was lifted from the chip. The unit was remounted in a DIC with silver epoxy, baked 2 hours at 200°C, rebonded and retested. VIO=0.46mV. Cause of out of spec CIO: marginal beam to chip contact.
	26	V-sense bench VIO=-9.4mV	512	After decap, 2 beams were lifted from the chip. The unit was remounted in a DIC with silver epoxy, baked 2 hours at 200°C, rebonded and retested. VIO=0.36mV. Cause of out of spec condition: marginal beam to chip contact.
	27	VIO=-8.3mV	128	After decap, 2 beams were lifted from the chip. The chip was remounted in a DIC with silver epoxy, baked 2 hours at 200°C, rebonded and retested. VIO=0.42mV. Cause of out of spec VIO: marginal beam to chip contact.
1B HRLC 225°C BL	57	Opens and shorts	256	Plastic at chip surface was insoluble due to excessive temperature. Probable cause: reversed insertion at testing.

Table IV-27

CA741 (Cont'd)

NAVELEX DEVICES ANALYSIS RESULTS (cont'd)

CELL	UNIT NO.	OUT OF SPEC PARAMETER	TEST HOURS	SUMMARY OF ANALYSIS
1C HRLC 200°C BL	87	VIO=+12mV		Pincheck showed pin 9 (offset) shorted to pin 6 (V-). Mechanically removing insoluble plastic from the chip; multiple arcover sites were observed between the parallel metal runs from pins 6 and 9. Cause of short: electrical overstress.
1F HRLC 250°C SL	175	VIO=-9.42mV		Pincheck showed pin 10 open. On decap, pin 10 had continuity; the open reading was probably due to oxidation on the external lead. However, after decap, other beams lifted from the chip. The chip was remounted in a DIC with silver epoxy, baked 2 hours at 200°C, rebonded and retested. VIO=1.6mV. Cause of out of spec condition: high resistance on pin 10 due to oxidation.
2D DIP Wire Bond 175°C BL	406	VIO=-17.6mV	8	Active probing showed capacitor C-1 shorted; cause: voltage overstress.
2E DIP Wire Bond 150°C BL	429	VIO=-17.6mV	1500	Damaged during decap process.
3A DIC 250°C BL	601	VIO=-17.6mV	2	Active probing showed capacitor C-1 shorted. Cause: short duration voltage overstress.
3B DIC 225°C BL	643	VIO=-17.6mV	4	Pin check showed open pin 10. Post delid visual showed wire bond lift at package pad.
3C DIC 200°C BL	673	Open pin 11	128	Post delid visual showed bond wire shear at heel of the chip bond.
3D DIC 175°C BL	697	VIO=+12mV	1008	After delidding and storage at room temp. VIO decreased to 0.07mV. Cause of out of spec condition: annealable mobile charge in or on the surface dielectric.
3G DIC 225°C SL	801	VIO=12mV	256	Bench VIO=+16.8mV (clamp value). Active probing with the op amp functioning on the VIO mode showed several voltage nodes in the output stage different than a standard reference 741. Two point probing across Q22/Q23 E-B showed a resistance of 1K ohms instead of 300K ohms. Using the protect puncture and etch isolation method, the individual Q22 and Q23 devices were probe tested and found normal. Possibly the anomalous site was etched away in the isolation process. Cause of out of spec VIO: not determined.

4. Causes of Failure - Conclusions

CA741

As seen in Fig. IV-37(a), the major category of failure was assembly-related with a predominant subcategory of beam lifts at the chip. Since the CD4012's analyzed had no beam lifts, the 741 lifts should be considered as a correctable, mechanically oriented problem, not a metallurgical problem.

CA4012

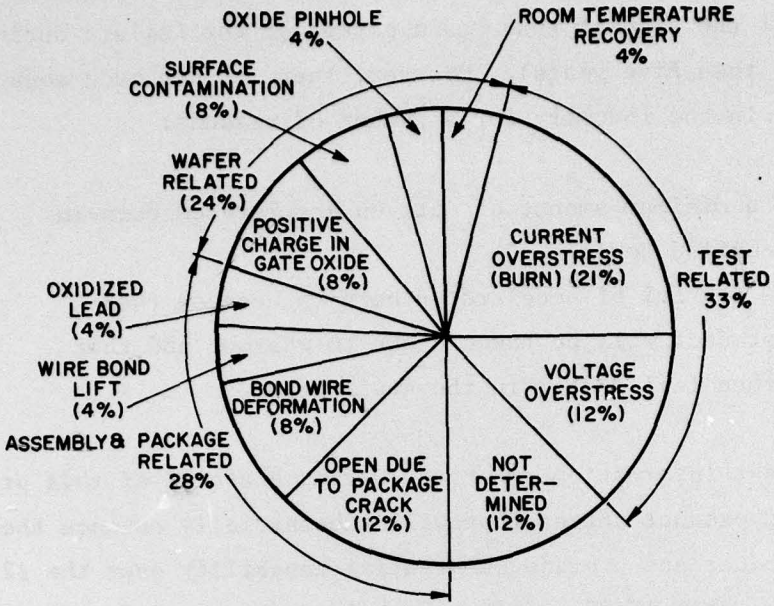
As shown in Fig. IV-37(b), the major categories were roughly evenly divided between package, wafer, and test related causes.

Compared to 741's analyzed, the CMOS units analyzed had a somewhat greater percentage of wafer and test related causes. Test engineering has indicated that programming more protective test procedures is feasible.

In contrast to the 741, the 4012 package-related causes were different: the ceramic package (DIC) cracks, and deformed bond wires on the non-sealed DIC's, were predominant subcategories. These are correctable, operator-training problems.

G. HRLC Screen

The ineffectiveness of 125°C, 168-hour burn-in for high-reliability product is well known. Although these conditions do remove some gross failures, most of the infant mortality is still present for the system to remove. Activation energies for the infant mortality generally range from 0.4 to 0.7 electron-volt depending on the predominant failure mechanism in the product.



(a) CD4012

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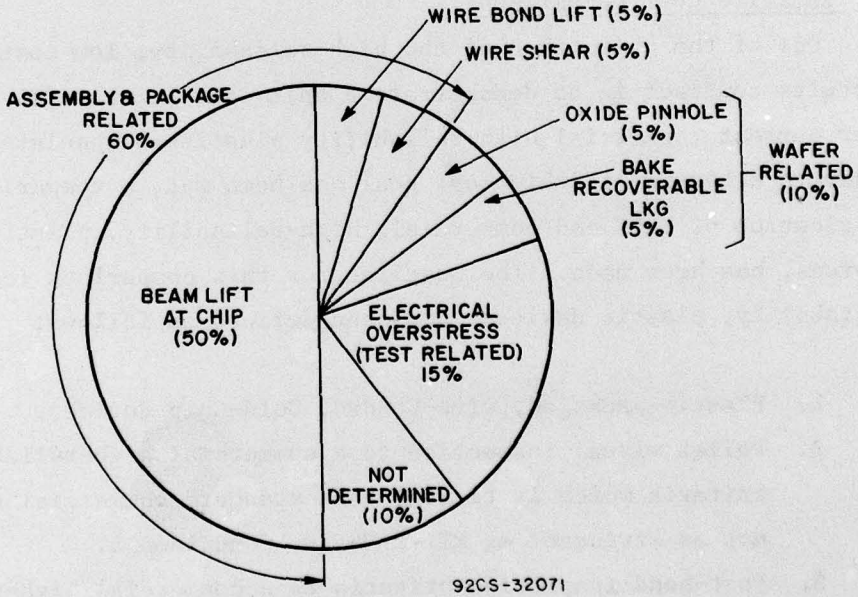

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(b) CA741

Fig. IV-37 - Phase-II summary charts of causes of failure.

It is generally acknowledged that burn-in at higher temperature eliminates more of the product that has a potential for failure during long system life (more than five years). However, there is not much acceptance of this technique in the industry for a number of reasons:

1. There is a minimum amount of data on accelerated burn-in for a specified device.
2. Users are fearful of accelerated burn-in because they believe product will be taken close to wearout and that it will then fail faster in the application.

The stress test information generated during Phase II of this program led to a proposed HRLC product screen that will substantially enhance the reliability of the product and provide substantial capability over the 125°C life data. As shown in Table IV-28, minimum burn-in temperature for HRLC product will be 150°C.

H. Relative Cost Comparison

One of the objectives of the high-reliability, low-cost, integrated-circuits contract is to demonstrate a unit cost increase of no more than 20% over current commercial high-reliability plastic-encapsulated devices. In order to determine if this cost goal has been met, a comparison, based on the fabrication of HRLC and commercial, high-reliability, plastic-encapsulated devices, has been made. The baseline for this comparison (commercial, high-reliability, plastic devices) has been defined as follows:

1. Plastic-packaged, wire-bonded, Gold-Chip devices.
2. Pellet visual inspection to a commercial high-reliability criteria which is tighter than standard commercial criteria but not as stringent as MIL-M-38510, Condition B.
3. Post-bond inspection criteria to a commercial high-reliability criteria which is tighter than standard commercial criteria but not as stringent as MIL-M-38510, Condition B.
4. Parts are burned in for 168 hours at 125°C.

Table IV-28 - Proposed HRLC Screen*

Stabilization Bake:	175°C 16 Hours
Temperature Cycle:	-65°C to 150°C 10 Cycles
Electrical Test:	25°C
Burn-In:	Dynamic Life Conditions
	150°C
	168 Hours
Electrical Test:	-55°C, 25°C, and 125°C

*Phase III devices, deliverables and those required for reliability verification testing, will be subjected to this screen.

Table IV-29 delineates the cost comparison for both domestic and offshore assembly locations using as a base the cost of a standard commercial device assembled offshore and available from distributor stock (line 1, Table IV-29). The cost adders for commercial high-reliability inspection, Q-line, (line 2) and burn-in (line 4) are shown separately. The base to which HRLC devices are to be compared is the sum of these three costs (lines 1, 2, and 4).

The relative cost for an HRLC device not burned in is shown on line 6. This device has the following attributes:

1. Silicon nitride chip passivation
2. Titanium-platinum-gold metallization
3. Plasma-deposited silicon nitride overcoat
4. Gold bonding bumps
5. Beam-tape bonding
6. Silicone molding compound
7. Class B inspections

The burn-in adder (line 7) for HRLC parts incorporates a 168-hour, 150°C ambient-temperature dynamic burn-in and post burn-in testing to MIL limits at -55°C, +25°C, and +125°C. The total HRLC relative cost is shown on line 8.

The cost of the commercial high-reliability plastic and HRLC devices may be compared by dividing line 5 by line 8. This comparison is shown on line 9. The table shows that for the case of offshore assembly, HRLC product costs are 15.4% higher than those of a commercial high-reliability device and, in the case of domestic assembly, the cost of commercial high-reliability plastic and HRLC devices is essentially the same. Analysis of the data indicates that, for U.S. assembly, the reduced labor costs associated with the beam tape system offsets the increased cost associated with Class B inspections. In the case of offshore assembly, where labor rates are an order of magnitude lower than in the U.S., the cost of the Class B inspection is only partically offset, resulting in the cost

Table IV-29 - HRLC Relative Cost Comparison

		Offshore Assembly	U.S. Assembly
1.	Standard	1.0	3.078
2.	Q-Line Adder	.067	.537
3.	Total Q-Line	1.067	3.615
4.	Burn-In Adder	.391	1.165
5.	Q-Line with Burn-In	1.458	4.780
6.	Class B Auto Dip	1.195	3.276
7.	Burn-In Adder	.488	1.454
8.	Total HRLC	1.683	4.730
9.	HRLC/Q-Line + Burn-In	1.154	.99

increase for HRLC devices. In either case, however, the cost goals of the contract have been achieved.

SECTION V

RCA GOVERNMENT CONTRACTS UTILIZING CONTRACT RELATED TECHNOLOGY

Sealed Chip Tape Carrier Program, USAERADCOM, Fort Monmouth, N.J. Contract No. DAAK20-79C-0258.

SECTION VI
PHASE III PROGRAM

Phase III of the HRLC contract is intended to demonstrate the reliability of the parts fabricated during Phase II. The test plan is delineated in Table VI-1. Down periods for the various tests are given in Table VI-2.

Prior to submitting units to testing in Phase III, the sequence below is followed to maximize the data obtained from the program.

1. Serialize, test and data-log units at -55°C, +25°C and +125°C ambient.
2. Dynamic burn-in at 150°C for 168 hours.
3. Test and data-log at -55°C, +25°C and +125°C ambient.

This procedure provides the data base to which future down-period readings can be compared in the study of parametric shifts.

The life tests delineated in Table VI-1 will allow the prediction of the failure rate at 125°C. The moisture, sequence, and thermal shock tests will establish the package integrity and the ability of the devices to withstand severe environmental conditions.

In addition to the devices required for the Phase III test program, units are also being tested and burned in for delivery to NOSC for other studies. The quantities of devices to be delivered are given in Table VI-3.

Table VI-1 - Phase III Program

SCREENED UNITS

LIFE TESTS

Operating Life
CA741, 5420, 54S20, 5470, 5472

Temp (°C)	HRLC DIP
125	150

Operating Life
CD4012, CD4027, CD4014

Temp (°C)	HRLC DIP
125	300

STATIC LIFE
CD4012, CA741, 54S20

Temp (°C)	HRLC DIP	HRLC DIC
150	30	30
175	30	30
200	30	30
225	30	30
250	30	30

STORAGE LIFE
CD4012, CA741, 54S20

Temp (°C)	HRLC DIP	HRLC DIC
150	25	5

MOISTURE TESTS*

Humidity-Bias

Conditions	HRLC DIP	HRLC DIC
85°C/85% EH	45	15

Presure Cooker

Conditions	HRLC DIP	HRLC DIC
15 PSIG	30	10

SALT ATMOSPHERE

Conditions	HRLC DIP	HRLC DIC
MIL 1009.1	20	10

THERMAL CYCLE TESTS*

Thermal Shock

Conditions	HRLC DIP	HRLC DIC
-65°C to +150°C (Liq.-to-Liq.)	20	5

TEMPERATURE CYCLE

Conditions	HRLC DIP	HRLC DIC
-65°C to +150°C (Air-to-Air)	20	5

SEQUENCE TESTS*

24-Hour Salt Atmosphere Plus 160-Hour 85°C Static Life

HRLC DIP	HRLC DIC
15	5

50-Cycle -65°C to +150 Thermal Shock Plus 160-Hour 125°C Operating Life

HRLC DIP	HRLC DIC
20	5

15-Cycle, -65°C to +150°C Thermal Shock Plus 10-Cycle -65°C to +150°C Temperature Cycle Plus 10-Day Moisture Resistance

HRLC DIP	HRLC DIC
20	10

*MOISTURE, SEQUENCE, and THERMAL CYCLE TESTS will be conducted on a 4 type mix in quantities shown; types: CA741, CD4012, 54S20, CD4014.

Table VI-2 - Schedule of Downtimes, Phase III

Test		Downtimes for Electrical Test
Operating Life	125°C	168,1000,2000,5000 Hours
Static Life	150°C	168,500,2000,5000 Hours
Static Life	175°C	168,500,2000,5000 Hours
Static Life	200°C	48,168,250,500,1000,2500 Hours*
Static Life	225°C	48,168,250,500,1000,2500 Hours*
Static Life	250°C	12,48,96,168,500,1000 Hours*
Storage Life	150°C	168,500,2000,5000 Hours
Humidity Bias Life	85°C/85% RH	168,500,1000,2500,5000 Hours
Pressure Cooker		48,96,200 Hours
Salt Atmosphere		24,96 Hours
Thermal Shock -65°C to 150°C		100,500,1000,2000 Cycles
Temperature Cycle -65°C to 150°C		100,500,1000,2000 Cycles
Sequence Test 1		1,2,3 Cycles
Sequence Test 2		1,2,3 Cycles
Sequence Test 3		1,2,3 Cycles

Note: Sequence tests are as follows:

1. Salt atmosphere plus bias life.
2. Thermal shock plus operating life.
3. Thermal shock plus temperature cycle plus moisture resistance.

*Tests to be extended to 50% failure point.

Table VI-3 - Deliverable Parts

Type	Quantity
CD4012	1500
CD4014	4000
CD4027	4000
CA741	2000
5420	4000
54S20	800
5470	3400
5472	1600

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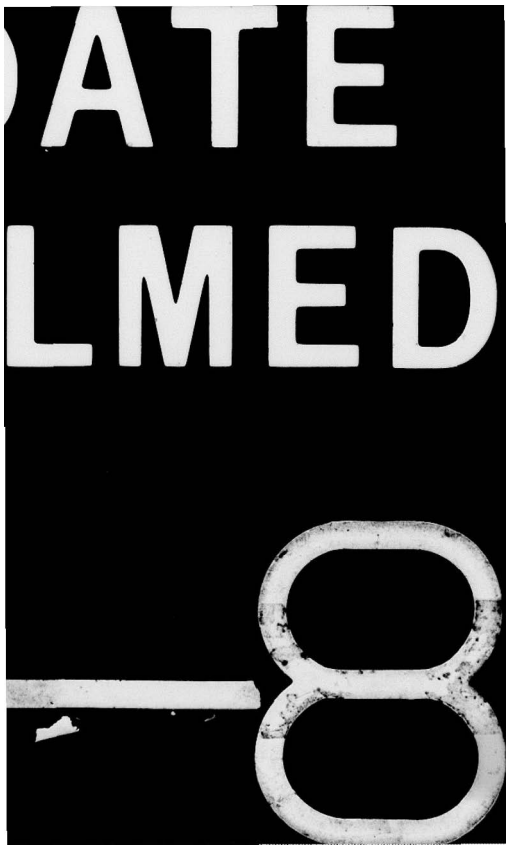
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